CUSTOM INTEGRATED AMPLIFIER CHIP FOR VLF MAGNETIC RECEIVER

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Abstract

Electronic systems for collecting measurements in harsh, remote environments face special challenges that often require custom designs. These systems must have the power capacity, data storage, and robustness to record high fidelity data for many months with no human contact. In this work, an integrated preamplifier for a magnetic sensor is designed to satisfy the size, weight, power, temperature, and noise specifications for long term deployment in Antarctica. The low impedance magnetic antenna (1 Ω–1 mH) requires a low input impedance amplifier and operates in the VLF (Very Low Frequency) range (50 Hz–30 kHz). At these low frequencies, $1/f$ noise becomes the dominating issue that limits performance. Due to the higher $1/f$ noise corner of MOSFET devices, only bipolar-junction transistors (BJTs) must be used in noise-critical parts of the design. Because of recent interest in BJTs for their superior performance at high frequencies in the gigahertz range, they are becoming available in the fabrication processes for integrated chips. With these new opportunities for using BJTs in integrated designs, low frequency amplifiers used in low noise applications can be integrated for the first time. In this thesis, a low impedance custom amplifier is presented that was implemented in National Semiconductor Corporation's BiCMOS process which meets the impedance and temperature requirements while achieving 2 pA/$\sqrt{\text{Hz}}$ current noise in band with only 5 mW of power. This noise level corresponds to a magnetic field noise of 0.25 fT/$\sqrt{\text{Hz}}$ for the loop antenna that is used for this application. The amplifier is field tested at the South Pole, successfully collecting data suitable for science research.

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Introduction

1.1 Project Overview

Low frequency electromagnetic waves have long wavelengths and can travel far distances, both along the surface of the Earth and along the magnetic field lines up into the ionosphere. By observing these signals in the 50 Hz–30 kHz range, generated either by lightning or large transmitters, valuable information is obtained about lightning, the ionosphere, and the near-Earth space environment [40, 56]. Since there is so much manmade noise in this frequency range, and since shielding is difficult, the receivers used to detect these signals are often located in remote areas far from power lines, generators, and other electronics [32, 53]. One of the best locations of scientific interest is near the South Pole and other locations in Antarctica [18]. Since the mid-to-high latitude magnetic field lines of interest, and the electromagnetic waves that follow them, intercept the surface of the Earth near the South Pole, a receiver located there can detect signals generated in the Van Allen radiation belts [46, pp. 51-54], which is a region of near-Earth space of particular scientific interest.

For this dissertation, a magnetic receiver system was desired that is capable of detecting such signals in Antarctica by operating unattended for an entire year. Magnetic receivers are used to detect these waves instead of electric receivers because they have better noise performance at low frequencies. Also, they are less affected by nearby metallic structures and do not require a ground plane. The inhospitable

environment and lack of power source make it difficult to build durable equipment that is also sensitive. Additionally, all travel is done by airplanes specially fitted for landing on snow, making it very expensive to service these remote sites to replenish the power supply renewal or for maintenance.

The receiver system designed and constructed during the course of this work replaces an older system used at several Antarctic sites which were deployed in the early 1990s, described in [41]. By reducing the cost of deployment and maintenance, many more sites can be added to the program to provide a clearer picture of the natural electromagnetic wave environment near the South Pole. Because of all of the technological advances over the past 20 years since the older system was developed, the new system required a complete redesign to incorporate the currently available parts, resulting in a much more compact, low power design.

1.2 Magnetic Receiver System Redesign Goals

The previous system (described in detail in [41]) uses about 7 W of power during operation, and one of the major expenses of the research program is flying the fuel to these sites. Therefore, the first major goal for the redesign effort is to reduce the power so that the whole system can last for a year on a single set of batteries. With sufficient data storage, the new system can operate for a full year with no maintenance. Additionally, no extra power is used to heat the electronics, and instead the system must survive the much colder temperatures.

Next, the electronics in the old system are stored in a small heated hut that is shared with other projects. These huts are very expensive to build because all of the parts have to be flown to the remote receiver site, and then it takes several days for the construction. The number of sites is limited to only seven, but with a smaller receiver that could be deployed more quickly, the number of sites could be greatly expanded. Therefore, the second main goal of the system redesign is to reduce physical size so that each system can be deployed within several hours, and require only a single airplane trip. The temperature in Antarctica varies widely, and can swing from -15°C to -80°C, making it difficult for the batteries and electronics

to maintain their performance. However, if the electronics are buried only a few feet in the snow, the temperature stays near -55°C year round. With careful insulation, the electronics can be kept warm enough to function. Since the noise from digital electronics can interfere with the antenna's sensitivity, the small preamplifier will be buried directly under the antenna, while the digital box will be buried up to 200 ft away. Therefore, the whole system consists of an antenna, preamplifier box, cable, and digital box which includes the batteries.

The noise of the system ideally should be below atmospheric noise so that all interesting signals would be captured. However, the atmospheric noise can be as low as 120 fT/$\sqrt{\text{Hz}}$ at 80 Hz and 1.5 fT/$\sqrt{\text{Hz}}$ at 1 kHz [6]. Therefore the noise floor of the system should be less than 1 fT/$\sqrt{\text{Hz}}$ in order to detect all of the signals above the atmospheric noise floor.

These goals require a complete redesign of the analog, digital, and power supply of the system, as well as adding thermal insulation. This thesis describes the analog front end portion of the project, with emphasis on the preamplifier design.

In order to minimize the physical size and weight of the preamplifier, to meet the project goals described above, the preamplifier will be integrated onto a chip. The previous preamplifiers used in the old system used discrete parts, so this project is the first time the preamplifier is integrated onto a chip. Additionally, by reducing the numbers of parts and solder connections, the new preamplifier will be faster to build and will be more robust throughout the mechanical and temperature strain during shipping, deployment, and operation.

1.3 Previous Magnetic Sensors

There are a variety of magnetic sensors currently available for both research and commercial use. The sensors most relevant for this project are presented below. Typically these designs are not constrained by our strict power, sensitivity, and weight requirements, hence they are found to be unsuitable for this research project.

1.3.1 Magnetic Sensors in Neural Research

Traditionally, the measurement of the magnetic fields created by nerve signals was performed using a toroid and a high impedance amplifier with feedback [11]. This system does get fairly good noise performance with a 100 Ω input impedance, however the noise figure increases dramatically at lower source resistances. An older neuron detector [19] uses CMOS probes and preamplifiers to detect neural signals between 100 Hz to 6 kHz with an amplitude up to 500 μV. Since CMOS devices are very noisy below 1 MHz, a BiCMOS preamplifier with a 2.5 V supply for 1 μV nerve signals has been developed [39]. Additionally this design uses a high input impedance circuit and expects a 1 kΩ input resistance. Decreasing the input impedance further with this approach would result in serious instability issues.

Another solution which also uses a toroid described elsewhere [54]. Here a high input impedance amplifier with feedback is used, achieving 110 nA/$\sqrt{\text{Hz}}$ current noise at 1 kHz with a 1 Ω source impedance, which is much too large for this application. Additionally, no information was given on the power consumption, since it probably was not a design priority. Most current neural research with a noninvasive probe requires the use of a high input impedance system with a capacitive probe, for example [17] and [33]. Since the magnetic sensors have a low impedance, these neural sensors can not be used for this application.

1.3.2 SQUIDs

SQUIDs (Superconducting Quantum Interference Devices) are used to measure small magnetic fields using a small loop antenna. These sensors are designed for low frequencies (<10 kHz) and can achieve very low noise, usually in the range of 1 fT–50 fT (sample systems include [9], [1], [58], and [7]). One particularly relevant application of a SQUID sensor is for mapping of underground features of the Earth [30], achieving a noise level down to 50 fT/sqrt(Hz), which is still above the 1 fT/$\sqrt{\text{Hz}}$ needed for this research.

Since all of these devices require a very low operating temperature (0.3 K–77 K) to achieve the superconducting state, they require special cooling equipment and

liquid gas. A receiver system that is deployed in a remote location without access to external power can not accommodate the power consumption and weight to maintain the operating temperature, much less the supply of liquid gas. Additionally, this cooling equipment can cause noise problems in the range of 50–100 fT/$\sqrt{\text{Hz}}$ [36].

1.3.3 Low Frequency Magnetometers

An early magnetometer is described in [23] where a ferrite coil is used to detect fields at 15 mT between 1.6 kHz and 50 MHz. In 1980, a system of three concentric loops was developed to achieve sensitivities down to -200 dB Gauss/$\sqrt{\text{Hz}}$ (1 μT/$\sqrt{\text{Hz}}$) at 100 Hz [27]. Another magnetometer was developed without a transformer for a high resistance (4.12 kΩ) air coil, achieving 130 fT/$\sqrt{\text{Hz}}$ sensitivity at 20 Hz [10]. A more recent design achieves 40 fT/sqrt(Hz) with a ferrite core coil, using feedback for impedance matching [36]. However, none of these systems are low power, and feedback systems are less robust with large temperature changes.

Another group has created a similar system for sensing magnetic fields with a transformer between the sensor and the amplifier [44]. However, they use a high input impedance amplifier with feedback. The result is a system that works between 600 Hz and 210 MHz.

None of these sensors achieve the required sensitivity, and most are not low power or integrated. The best frequency response and noise performance is achieved when the input impedance is low, as discussed in Section 2.2.2. However, most amplifiers designed for the applications discussed above use a high impedance op-amp with feedback. As the input impedance is lowered, the stability requirements make this topology choice difficult to implement. Instead, building a current amplifier directly allows for better stability and control for desired gain parameters, as well as reducing the power consumption, and is the preferred choice for this dissertation.

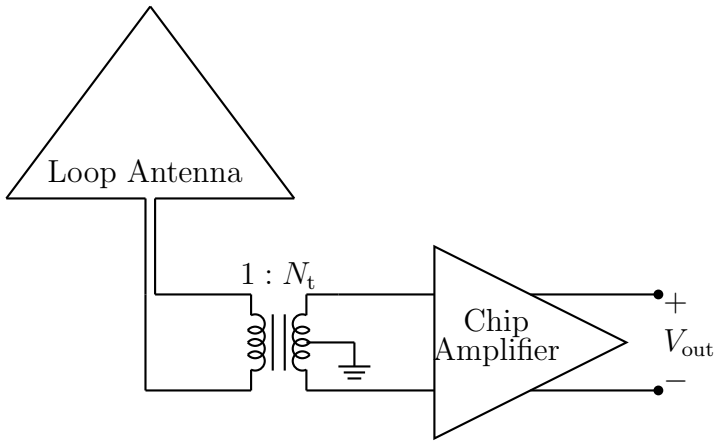

Figure 1.1: Front end of analog portion of receiver system including antenna, transformer, and amplifier. Full systems include two copies of the design with the antennas arranged orthogonally.

1.4 Analog Front End Overview

The analog front end of the receiver system includes the antenna, transformer, and amplifier, shown in Figure 1.1. Usually each system includes two channels that each have an antenna, transformer, and amplifier. The two antennas arranged orthogonally (often one is oriented in the north-south direction, and the other in the east-west). The data from the two channels can be used to determine the direction of arrival of the signals. For simplicity, only one channel is shown here. In ground-based magnetospheric research a large loop antenna is used to detect electromagnetic signals. A transformer steps up the signal voltage and DC isolates the antenna from the rest of the receiver. The antenna and transformer designs are discussed in Chapter 2.

The integration of the amplifier onto a chip significantly reduces the size and weight of the preamplifier, while reducing the soldering time for each board. However, a new amplifier design is required to meet the requirements in the new integrated environment. First, the receiver needs to have a flat frequency response over the bandwidth of the data, from 50 Hz to 30 kHz. If an amplifier with a low input impedance is used, the increase in induced voltage in the antenna with frequency is counteracted by the increase in inductive reactance of the antenna, making the

current into the receiver flat with frequency. Although many of the other magnetic amplifier designs discussed above use a high impedance amplifier with a shunt resistor to lower the input impedance, the thermal noise of the shunt resistor degrades the noise performance significantly, making it impossible to meet the noise requirement with a 1 Ω input impedance. Instead, an amplifier that is designed to have a low input impedance, without any shunt resistor, is required to meet the receiver specifications.

1.4.1 Amplifier Specifications

The specifications for the single chip amplifier are derived directly from the requirements of the project as a whole. The primary specification is the sensitivity because it determines whether scientifically interesting signals are detectable. With the 5 turn, 10 m base triangular antenna used for the receiver system, the 1 fT/$\sqrt{\text{Hz}}$ magnetic field noise specification corresponds to a 7.8 pA/$\sqrt{\text{Hz}}$ input current noise. A gain of at least 15 mV/nA is needed to ensure the signals are large enough to be digitized precisely. Since the batteries have to supply all the power for the system for a whole year, the power consumption of the parts is budgeted. Only 5 mW of power is available for the amplifier, which is a significant reduction from the 71 mW consumption in the preamplifier used in the old system. There are no commercially available integrated amplifiers that meet the power and sensitivity specifications, so a new custom amplifier is needed. Achieving these specifications for an integrated amplifier chip resulted in the contributions listed below.

1.5 Contributions

This work demonstrates the first integrated amplifier that meets the performance requirements for a VLF magnetic receiver. The amplifier achieves a 1.8 pA/$\sqrt{\text{Hz}}$ current noise midband, and remains below the 7.8 pA/$\sqrt{\text{Hz}}$ specification[1] between 234 Hz and 370 kHz. The gain also exceeds the specification between 90 Hz and 110 kHz, and reaches 35 mV/nA midband, while using less than 5 mW of power.

[1]Corresponds to 1 fT/$\sqrt{\text{Hz}}$ system sensitivity with a 5 turn, 10 m base triangular antenna.

Additionally, an optimization technique is developed to minimize the noise of the first stage, which can be used for any common base amplifier stage. The chip amplifier was field tested in Antarctica in a fully autonomous system and produced scientifically useful data for a year. A summary of the main contributions is listed below:

- Design of an integrated amplifier that meets the performance requirements for a VLF magnetic receiver.
- Development of noise optimization for bias current in a common-base topology.
- Implementation of the integrated amplified that achieves 1.8 pA/$\sqrt{\text{Hz}}$ of current noise and 35 mV/nA of gain while using 4.8 mW of power.

1.6 Dissertation Organization

This dissertation presents the design and testing of the integrated amplifier as follows. Chapter 2 provides some necessary background on the antenna and transformer design, along with the basic relationships and noise characteristics of transistors. The design specifications and challenges is described in Chapter 3, and the design work to satisfy them is presented in Chapter 4. The noise optimization of the first stage is also included in the design chapter. Chapter 5 describes the testing methods and Chapter 6 presents the amplifier performance results. The integration of this amplifier into the rest of the magnetic sensor is discussed in Chapter 7, as well as the field test results. Finally, Chapter 8 provides the conclusions and suggestions for future work.

Chapter 2

Background

Before discussing the design of the amplifier and the rest of the analog portion of the system, the design of the antenna and transformer are presented. Their characteristics affect the noise performance of the entire system directly, so it is important to understand them well. A brief overview of the fundamental noise sources follows, and then finally the basic relationships of bipolar and MOSFET devices are reviewed.

2.1 Antenna Design

Magnetic field sensors are preferred at very low frequencies instead of electric field sensors mostly because they have superior noise response at the low end of the freqeuncy range. They are also less affected by nearby metallic structures and noise from snow, allowing for more accurate recording of the signal. Finally, magnetic field antennas do not require a ground plane, which simplifies their construction and calibration. The antenna and transformer designs were originally developed by Evans Paschal [35], and has been used in a large variety of low frequency magnetic receivers.

All magnetic antennas are constructed as a loop of wire, with either a high permeability (usually ferrite) core at the center, or nothing (air core). Antennas with a high permeability core are physically smaller, although not necessarily lighter, so they are often used where the space is the primary concern. However, their sensitivity can change with temperature, strong fields can cause a nonlinear response, and they

are more difficult to calibrate [35]. Since the systems for this project are deployed in remote areas where the antenna size is not limited, large air core antennas are constructed and used on site.

The model for the antenna is shown in Figure 2.1, along with the transformer and amplifier. The voltage source, V_a, represents the induced voltage in the loop from the magnetic field. The inductor L_a represents the coil inductance, and the resistor R_a is the parasitic wire resistance.

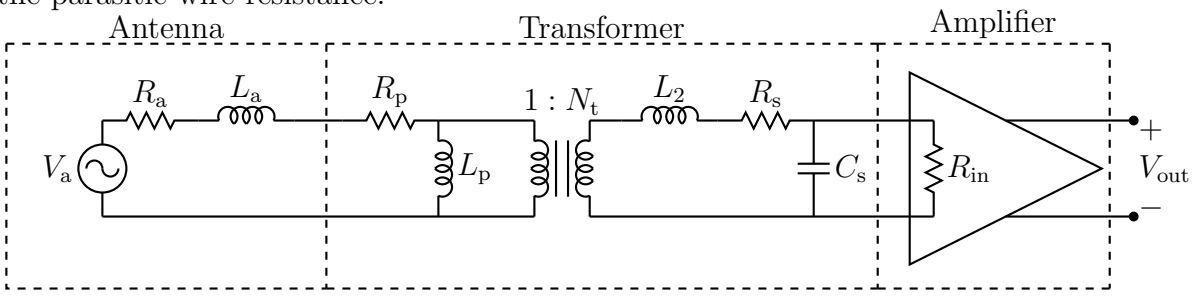

Figure 2.1: System design of fully differential magnetic field receiver including antenna model, transformer model, and amplifier input impedance

2.1.1 Antenna Sensitivity

When designing an air loop antenna, there are three critical parameters: the area of the antenna A_a, the diameter of the wire d, and the number of turns N_a. These parameters determine the antenna wire resistance, R_a, and inductance, L_a, which in turn shape the system response and sensitivity. The winding capacitance and skin effect are negligible at frequencies below the megahertz range. It is therefore important to derive the relationship among the three parameters and the resulting sensitivity.

The loop shape is usually chosen based on its ease of construction and the desired area. A variety of common loop shapes are listed in Table 2.1. The constant c_1 is related to the geometry of the antenna and allows for a general expression of the length of each turn that is valid for any shape:

$$\text{Antenna Turn Length} = c_1\sqrt{A_\mathrm{a}} \tag{2.1}$$

Shape of Loop	c_1	c_2
circular	3.545	0.815
regular octagon	3.641	0.925
regular hexagon	3.722	1.000
square	4.000	1.217
equilateral triangle	4.559	1.561
right isosceles triangle	4.828	1.696

Table 2.1: Constants for various magnetic loop antenna shapes

Using this expression, the antenna resistance for any shape is

$$R_{\mathrm{a}} = \frac{4\rho N_{\mathrm{a}} c_1 \sqrt{A_{\mathrm{a}}}}{\pi d^2} \tag{2.2}$$

where ρ is the resistivity of the wire (for copper, $\rho = 1.72 \times 10^{-8}$ Ωm) and d is the diameter of the wire. Adapting from [47, pp. 49-53], the inductance for any loop antenna is

$$L_{\mathrm{a}} = 2.00 \times 10^{-7} N_{\mathrm{a}}^2 c_1 \sqrt{A_{\mathrm{a}}} \left[\ln \frac{c_1 \sqrt{A_{\mathrm{a}}}}{\sqrt{N_{\mathrm{a}}} d} - c_2 \right] \tag{2.3}$$

where c_2 is also a geometry related constant, and can be found in Table 2.1 for a variety of loop shapes. The two variables R_{a} and L_{a} form the total impedance of the antenna (Z_{a}) that is the source impedance seen by the first stage of the receiver.

$$Z_{\mathrm{a}} = R_{\mathrm{a}} + j\omega L_{\mathrm{a}} \tag{2.4}$$

When an incident electromagnetic wave passes through the antenna, the voltage induced across its terminals is given by Faraday's Law:

$$V_{\mathrm{a}} = j2\pi f N_{\mathrm{a}} A_{\mathrm{a}} B \cos(\theta) \tag{2.5}$$

where V_{a} is the voltage signal magnitude, f is the frequency, B is the magnetic flux density, and θ is the angle of the magnetic field from the axis of the loop. If the axis of the loop is horizontal, the response pattern of the antenna is a dipole in azimuth.

For simplicity in the following design discussion, the field is assumed to be oriented normal to the antenna, and the term $\cos(\theta)$ is omitted.

Since the size of a VLF receiving loop is very small compared to a wavelength (λ=1000 km at 300 Hz and 10 km at 30 kHz), the radiation resistance of the loop is negligible compared to the wire resistance R_{a}. Therefore, the minimum detectable signal is limited by the thermal noise of R_{a}. The sensitivity of the antenna, S_a, is defined as the field equivalent of the noise density; that is, the amplitude of an incident wave which would produce an output voltage equal to the thermal noise of R_a in a 1 Hz bandwidth. Using equation (2.5) the sensitivity (in units of T/Hz$^{1/2}$) can be expressed as:

$$S_{\mathrm{a}} = \frac{\sqrt{4kTR_{\mathrm{a}}}}{2\pi f N_{\mathrm{a}} A_{\mathrm{a}}} \tag{2.6}$$

Note in equation 2.6 that the antenna sensitivity S_{a} decreases with frequency (that is, the antenna becomes more sensitive). It is convenient to define a frequency-independent quantity for comparing the performance of different antennas, thus the normalized sensitivity is defined as $\hat{S}_{\mathrm{a}} = fS_{\mathrm{a}}$. Using R_{a} in equation (2.2), we find an expression for the normalized sensitivity that depends only on the physical parameters of the antenna:

$$\hat{S}_{\mathrm{a}} = \frac{\sqrt{4kT\rho c_1}}{\pi^{3/2} d\sqrt{N_{\mathrm{a}}} A_{\mathrm{a}}^{3/4}} \tag{2.7}$$

This expression for sensitivity can be used to find the number of turns, antenna area, and wire diameter required for a target sensitivity at a specific frequency. The effect of the resulting antenna resistance and impedance on the rest of the system is discussed in later sections.

Further insight can be gained by expressing this sensitivity as a function of the mass of the antenna. The mass of the wire used in the antenna is found to be:

$$M = \frac{1}{4}\pi\delta c_1 d^2 \sqrt{N_{\mathrm{a}}} \tag{2.8}$$

where δ is the density of the wire. Solving this for $d\sqrt{N_{\mathrm{a}}}$ and substituting into (2.7)

produces normalized sensitivity:

$$\hat{S}_{\mathrm{a}} = \frac{c_1\sqrt{4kT\rho\delta}}{2\pi\sqrt{MA_{\mathrm{a}}}} \tag{2.9}$$

This interesting result shows that the only way to improve sensitivity with a given antenna material is to increase the total mass or area of the antenna. By expressing $\sqrt{A_{\mathrm{a}}}$ in terms of the mass, the dependence of the sensitivity on the mass of the antenna is made clear:

$$\hat{S}_{\mathrm{a}} = \frac{c_1^2 d^2 \delta\sqrt{4kT\rho\delta}}{8M^{\frac{3}{2}}} \tag{2.10}$$

This equation shows that the mass of the antenna is the fundamental tradeoff for the antenna sensitivity. Magnetic sensors are usually placed in remote areas to reduce interference from power lines (at 60 Hz and harmonics), so this tradeoff means that the sensitivity must be balanced against the practical weight limitations in shipping and construction of the antennas. The most severe limitations for these receivers are for units placed at the South Pole for research on electromagnetic waves in near-Earth space and the radiation belts. Since the Earth's magnetic field lines that pass through these regions in the upper atmosphere intercept the surface of the Earth near the polar regions, a ground-based receiver at the South Pole can detect the very low frequency signals of interest, while also taking advantage of the pristine low-noise environment due to the lack of other (man-made) noise sources.

2.2 Transformer

The transformer electrically isolates the antenna from the rest of the receiver and steps up the impedance by a factor of the turns ratio squared, N_{t}^2, to improve the impedance match to the preamplifier. Also, the low frequency cut-off of the transformer reduces the noise from the system at frequencies below those of interest. Figure 2.1 shows the circuit model for the transformer and the other equivalent noise sources from the amplifier.

2.2.1 Transformer Frequency Response

The combined transfer function of the antenna and transformer that relates the input voltage of the amplifier, V_{in}, to the induced voltage of the antenna, V_{a}, can be found with standard circuit analysis:

$$\frac{V_{\mathrm{in}}}{V_{\mathrm{a}}} = \frac{jwN_{\mathrm{t}}L_{\mathrm{p}}R_{\mathrm{in}}}{k_1k_2 + k_3} \tag{2.11}$$

where

$$\begin{aligned} k_1 &= [R_{\mathrm{a}} + R_{\mathrm{p}} + jw(L_{\mathrm{a}} + L_{\mathrm{p}})] \\ k_2 &= [(R_{\mathrm{s}} + jwL_2)(1 + jwC_{\mathrm{s}}R_{\mathrm{in}}) + R_{\mathrm{in}}] \\ k_3 &= jwL_{\mathrm{p}}N_{\mathrm{t}}^2(R_{\mathrm{a}} + R_{\mathrm{p}} + jwL_{\mathrm{a}})(1 + jwC_{\mathrm{s}}R_{\mathrm{in}}) \end{aligned}$$

Using equation 2.5 to relate the amplifier input voltage, V_{a}, to the incident magnetic field, B, and simplifying, results in the approximate equation shown below.

$$V_{\mathrm{in}} \approx \frac{N_{\mathrm{a}}A_{\mathrm{a}}R_{\mathrm{in}}B}{N_{\mathrm{t}}(L_{\mathrm{a}} + pL_2/N_{\mathrm{t}}^2)} \left[\frac{f}{f - jf_{\mathrm{t}}}\right] \left[\frac{f}{f - jf_{\mathrm{i}}}\right] \left[\frac{-jf_{\mathrm{c}}}{f - jf_{\mathrm{c}}}\right] \tag{2.12}$$

where

$$\begin{aligned} f_{\mathrm{t}} &= \frac{(R_{\mathrm{a}} + R_{\mathrm{p}})||[(R_{\mathrm{s}} + R_{\mathrm{in}})p/N_{\mathrm{t}}^2]}{2\pi(L_{\mathrm{a}} + L_{\mathrm{p}})} \\ f_{\mathrm{i}} &= \frac{R_{\mathrm{a}} + R_{\mathrm{p}} + (R_{\mathrm{s}} + R_{\mathrm{in}})p/N_{\mathrm{t}}^2}{2\pi(L_{\mathrm{a}} + pL_2/N_{\mathrm{t}}^2)} \\ f_{\mathrm{c}} &= \frac{1}{2\pi C_{\mathrm{s}}R_{\mathrm{in}}} \\ p &= 1 + L_{\mathrm{a}}/L_{\mathrm{p}} \end{aligned}$$

The various factors that have been isolated facilitate the understanding of how the transfer function is affected by both the design of the transformer and the input impedance of the amplifier. The factor p is the ratio of the total inductance on the

primary side (including the antenna and L_p) to the transformer primary inductance alone (L_p). For an ideal transformer, L_p=∞, and p=1. Below the frequency f_t, the shunting effect of L_p becomes important and the gain drops rapidly. The receiver is not useful in this region, making f_t the low frequency limit of the receiver response.

The input turnover frequency f_i is the frequency where the total resistance in the input circuit equals the inductive reactance. Note that f_i is much higher than f_t in a good design. Above f_i the impedance of the input circuit is dominated by the antenna inductive reactance $2\pi f L_\mathrm{a}$. Even though the induced voltage across the antenna terminals (2.5) is proportional to frequency, the current in the input circuit above f_i is limited by the antenna reactance, which also increases with frequency, giving the output signal a flat overall frequency response. The wide bandwidth with a flat response simplifies the study of signals such as spherics and whistlers that span several decades of frequency.

At the frequency f_c the transformer secondary shunt capacitance C_s begins to short the input signal and the gain drops. The interval of flat frequency response is thus from f_i to f_c. Note that the transformer leakage inductance L_2 does not significantly affect performance, because it appears in series with the much larger $N_\mathrm{t}L_\mathrm{a}$, as seen on the secondary side of the transformer.

2.2.2 Transformer Effects on System Noise

The main sources of noise in the system are the thermal noise of the antenna ($\overline{v_\mathrm{na}^2}$), voltage noise of the amplifier ($\overline{v_\mathrm{n,amp}^2}$), and the current noise of the amplifier ($\overline{i_\mathrm{n,amp}^2}$) (see Section 2.4.4 for amplifier noise model). The system sensitivity is directly affected by the transformer turns ratio and the ratio of current and voltage noise of the amplifier. For an ideal transformer:

$$S_\mathrm{sys} = \frac{\overline{v_\mathrm{na}^2} + \overline{v_\mathrm{n,amp}^2}/N_\mathrm{t}^2 + \overline{i_\mathrm{n,amp}^2}N_\mathrm{t}^2 Z_a^2}{\omega N_\mathrm{a} A_\mathrm{a}} \tag{2.13}$$

Since the effect of the amplifier noise voltage is reduced by the transformer turns ratio while that of the noise current is increased, the choice of turns ratio has a direct effect on the sensitivity. Typically N_t is chosen so that R_a=$R_\mathrm{in}/N_\mathrm{t}^2$. In other words,

the turns ratio is chosen to make the input impedance of the amplifier, as seen at the transformer primary, about the same as the antenna resistance in order to balance the low and high frequency noise concerns. With a common-base input stage, this turns ratio also means that $\overline{v_{\rm na}^2} \simeq \overline{v_{\rm n,amp}^2}/N_{\rm t}^2$, thus making the low-frequency noise of the amplifier about the same as the thermal noise of the antenna. With this choice, the sensitivity improves with higher frequency for a decade or two above $f_{\rm i}$ until current noise $\overline{i_{\rm n,amp}^2}$ flowing through $N_{\rm t}^2 Z_{\rm a}^2$ becomes important and the sensitivity levels off. Note that a common-base input stage of input resistance $R_{\rm in}$ gives much better noise performance than an actual resistor of size $R_{\rm in}$, even if followed by a noiseless amplifier. The reason is that the current noise of the common-base circuit is much lower than the Johnson thermal current noise of the real resistor.

However, a real transformer adds some noise and changes the response. When the components $L_{\rm p}$, $R_{\rm p}$, L_2, and $R_{\rm s}$ (as shown in Figure 2.1) are included, the total input referred voltage noise is:

$$\begin{aligned}\overline{v_{\rm n,tot}^2} \approx & \overline{v_{\rm na}^2} + \overline{v_{\rm n,p}^2} + \frac{\overline{v_{\rm n,s}^2}}{N_{\rm t}^2} p^2 \left(1 + \frac{f_{\rm tn}^2}{f^2}\right) \\ & + \frac{\overline{v_{\rm n,amp}^2}}{N_{\rm t}^2} \left[\left(p - \frac{f^2}{f_{\rm cn}^2}\right)^2 + p^2 \frac{f_{\rm tn}^2}{f^2}\right] \\ & + I_{\rm n}^2 N_{\rm t}^2 R_{\rm a}^2 \left(1 + \frac{(2\pi f L_{\rm a})^2}{R_{\rm a}^2}\right)\end{aligned} \tag{2.14}$$

where

$$f_{\rm tn} = \frac{R_{\rm a} + R_{\rm p}}{2\pi(L_{\rm a} + L_{\rm p})}$$

$$f_{\rm cn} = \frac{1}{2\pi\sqrt{C_{\rm s} N_{\rm t}^2 L_{\rm a}}}$$

To find the sensitivity, convert the input referred noise to the equivalent field using the antenna parameters:

$$S_{\rm sys} = \frac{\overline{v_{\rm n,tot}}}{\omega N_{\rm a} A_{\rm a}} \tag{2.15}$$

Comparing this result to the sensitivity of only the antenna in equation (2.6), the

sensitivity of the system is similar in form to that of the antenna by itself, with the antenna noise being replaced by the combined total noise of the antenna, transformer, and amplifier, $\overline{v_{\mathrm{n,tot}}}$. At a given frequency, the receiver approaches ideal performance as the amplifier and transformer noise decreases toward the antenna thermal noise, $\overline{v_{\mathrm{na}}}$.

The transformer has several important effects on the overall noise. The most important is the thermal noise from series resistances in the transformer, R_{p} and R_{s}, which add directly to the system noise. These resistances must be kept as small as possible to minimize the impact on the rest of the system. At low frequencies $f^2/f_{\mathrm{cn}}^2 \rightarrow 0$ and the voltage noise is multiplied by the factor p. Therefore, for good low frequency noise performance, p must be kept small (i.e. L_{p} made large). Also, at frequencies below f_{tn}, the noise performance deteriorates rapidly, so f_{tn} must be kept small. At high frequencies, more of the amplifier voltage noise appears across the transformer capacitance C_{s} and increases the noise. So, for good high frequency noise performance, f_{cn} should be kept large.

2.3 Antenna and Transformer Parameters

The previous Sections describe how the antenna and transformer both influence each other and the performance of the system, demonstrating that they must be designed conjointly as a unit, along with the amplifier input characteristics. The particular design used for this project is discussed below.

2.3.1 Antenna Parameters

The antenna design must balance desired sensitivity with the practicality of construction. The resistance and inductance of the antenna from equations 2.2 and 2.3 affect the frequency response and sensitivity (2.12 and 2.15). A lower antenna resistance, R_{a}, results in lower noise and better sensitivity (see equation 2.13), but requires wire with a larger diameter which becomes increasingly heavier. Additionally, increasing

Base (m)	Wire AWG	N_a	R_a (Ω)	L_a (mH)	A_a (m^2)	$\hat{S}_a$ ($V\sqrt{Hz}/m$)
Square Antenna						
0.160	20	47	1.002	0.998	.02563	5.03×10^{-3}
0.567	18	21	1.006	0.994	.3219	8.96×10^{-4}
1.70	16	11	0.987	1.013	2.892	1.89×10^{-4}
4.90	14	6	0.972	1.029	24.05	4.13×10^{-5}
Right Isosceles Triangle						
2.60	16	12	0.994	1.005	1.695	2.97×10^{-4}
8.39	14	6	1.004	0.996	17.59	5.74×10^{-5}
10.0	14	5	0.999	0.975	25.00	4.84×10^{-5}
27.3	12	3	1.035	0.967	187.0	1.10×10^{-5}
60.7	10	2	0.959	1.043	920.9	3.22×10^{-6}
202	8	1	1.005	0.995	10164	5.97×10^{-7}

Table 2.2: Magnetic field antenna designs with 1 Ω–1 mH impedance. Two shapes are included, square and right isosceles triangle.

the number of turns (also increasing the weight), produces a larger antenna inductance, L_a, thereby increasing the induced voltage for a given field (equation 2.5) and improves sensitivity (2.13). For this design, a 1 Ω–1 mH antenna impedance is chosen. This impedance balances the need for sensitivity, with the weight and construction time limitations during deployment.

Using equations 2.2, 2.3 and 2.6 a family of copper-wire loops of various sizes and sensitivities can be found, all with the same impedance. These antennas, listed in Table 2.2 for a 1 Ω–1 mH impedance, can be interchanged and used with the same receiver depending on the sensitivity required. Similar tables can be constructed for other impedance choices. The smaller antennas are more portable while the large antennas are more sensitive, so the antenna size used for a particular receiver is dependent upon needed sensitivity and available physical space. For example, a small antenna can be used with a receiver system to determine the best, low-noise site to construct a permanent, large antenna. However, not only are large antennas heavy and difficult to erect in remote areas, wind can also cause vibrations that can be mistaken for data variations. Large antennas should use a stiff frame to keep wind

vibrations small. For large open triangular antennas supported by a central tower, the antenna wire should be kept slack so wind vibrations are below the frequencies of interest. For the measurements made in this dissertation, we used a five turn triangular antenna with a 10 m base which balanced the sensitivity and weight requirements, while the triangular shape simplified the construction.

2.3.2 Transformer Parameters

The primary focus for the transformer design is sensitivity. The turns ratio for the transformer, N_{t}, is 16 and the primary inductance, L_{p}, is 10 mH.[1] The high frequency response is dominated by the winding capacitance C_{s}, which is 950 pF in this case. This capacitance is high because bifilar winding is used in both the transformer primary and secondary windings to assure balanced coupling. Using single-strand winding, C_{s} can be much smaller.

The following parameters' values are calculated as described in equation 2.12.

$$\begin{aligned} p &= 1.10 \\ f_{\mathrm{t}} &= 7.62 \text{ Hz} \\ f_{\mathrm{i}} &= 320 \text{ Hz} \\ f_{\mathrm{c}} &= 1.24 \text{ MHz} \end{aligned} \tag{2.16}$$

The voltage at the input of the amplifier terminals compared with the input magnetic field is depicted in Figure 2.2. The system frequency range is limited at the low end by f_{t}, and at upper frequency by f_{c}, resulting in an available bandwidth of 7.62 Hz – 1.24 MHz, well outside the required 50 Hz – 30 kHz bandwidth for the project. Also, for the noise performance of the transformer, the low frequency noise corner f_{tn} is 14.5 Hz and the high frequency corner f_{cn} is 10.2 kHz.

[1] The transformers were designed and constructed by Dr. Evans Paschal.

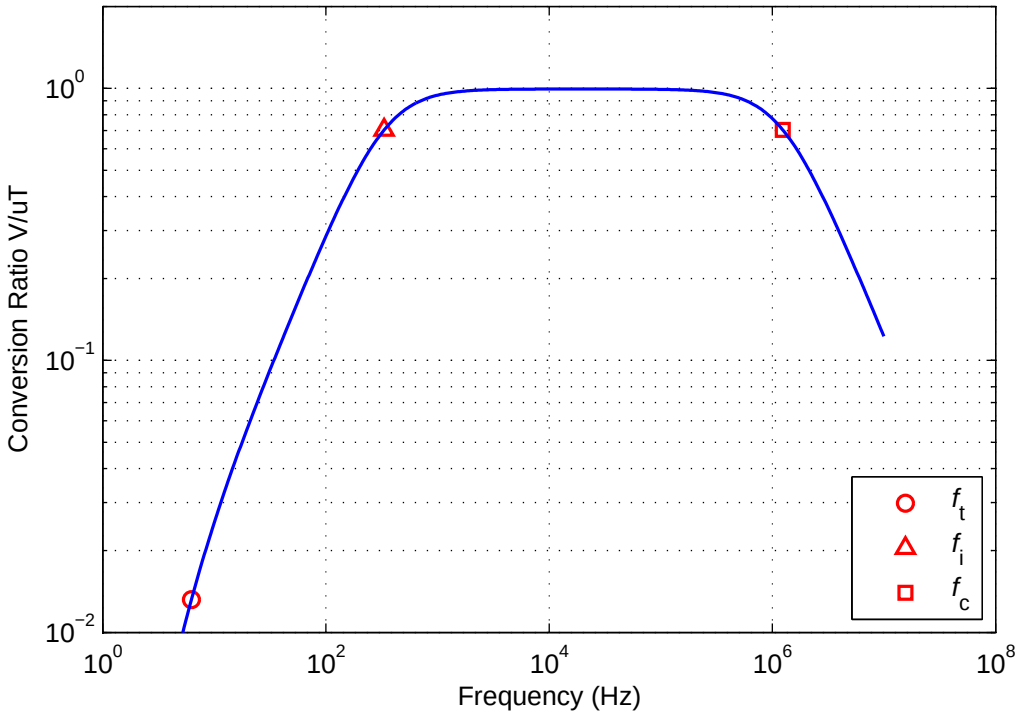

Figure 2.2: Frequency response of antenna and transformer combined. The three frequencies that determine the bandwidth of the system, f_t,f_i, and f_c, are depicted in red.

2.4 Noise Sources

Sensitivity is the most important specification for this amplifier, so the major noise sources that limit the sensitivity must be well understood. In this Section, we review the three main types of noise, all of which are present in the amplifier.

2.4.1 Thermal Noise

Thermal noise is generated by the random motion of electrons in any real resistor. The combined random motion of the electrons results in a noise current with the

following noise power (from [29, p. 10]):

$$\overline{i_{\mathrm{t}}^2} = kTf\frac{1}{R}\Delta f \tag{2.17}$$

where k is Boltzmann's constant (1.38 x 10^{-23} W-s/K), T is the temperature in Kelvin, Δf is the noise bandwidth, and R is the resistance. The noise power is constant for a pure resistor across the frequency spectrum (white noise). An equivalent voltage noise generated by the noise current is:

$$\overline{v_{\mathrm{t}}^2} = kTfR\Delta f \tag{2.18}$$

2.4.2 Shot Noise

Shot noise is generated from the random arrival times of electrons when they cross an energy barrier, such as a p-n junction. It occurs in any device with a p-n junction such as diodes and all types of transistors. The noise power is also flat over frequency and is directly related to the DC current flowing through the junction ([29, p. 28]).

$$\overline{v_{\mathrm{shot}}^2} = 2qI_{\mathrm{DC}}\Delta f \tag{2.19}$$

where q is the charge of an electron (1.6 x 10^{-19} coulomb).

2.4.3 Flicker Noise

Flicker, or $1/f$ noise, inversely proportional to frequency, so it is referred to as "pink" noise. It is present in all transistors and some resistors when they have DC current flowing through them.

The origin of the noise has been under dispute. Some claim it is quantum in nature [14] and stems from the interaction of charge carriers with the photons they emit from lattice scattering. Although the $1/f$ noise relationship to the mobility can be explained this way, the most recent experimental evidence indicates that when the

lattice is damaged, the $1/f$ noise increases, while the mobility does not correspondingly change [16]. This evidence points to surface traps that capture charge carriers for a random amount of time and the bulk recombination of that charge [50] and [57]. The time constants of the release from the traps and the recombination generate the $1/f$ noise spectrum that increases with each lower decade of frequency [13] and [20].

The noise power is related both to the DC current density and characteristics of the fabrication of the device. The $1/f$ noise is in all forward biased p-n junctions, which in a BJT is the base-emitter junction. A common estimate of this noise is shown below [29, pp. 113-114]

$$\overline{i_{\mathrm{f}}^2} = \frac{K\Delta f}{f}\frac{I_{\mathrm{B}}}{A_{\mathrm{j}}} \tag{2.20}$$

where A_{j} is the area of the junction, f is the frequency, and the factor K is a constant empirically related to a particular fabrication process. The ratio of DC base current to the junction area implies the noise depends on the current density within the device. The current and physical size of the devices are the only means a designer has in reducing the $1/f$ noise of a device in a particular process, so it is important to choose a process with devices that have acceptable $1/f$ noise performance.

There is also $1/f$ noise in integrated resistors, and the noise power follows this relationship from [25, p. 254]:

$$\overline{i_{\mathrm{f}}^2} = \frac{KV^2\Delta f}{f}\frac{R_{\square}^2}{A} \tag{2.21}$$

where V is the DC voltage across the resistor DC and $R_{\square}$ is the sheet resistivity.

A common way to compare the flicker noise in a device is to measure the "noise corner" frequency. This frequency is the point when the flicker noise equals the other white noise of the device from thermal and shot noise sources. Above this point the thermal and/or shot noise dominates, while at frequencies below this point the flicker noise dominates. When designing circuits for low frequency applications, it is especially important to chose devices with a low flicker noise corner frequency, and if possible, the flicker noise corner should be below the frequencies of interest.

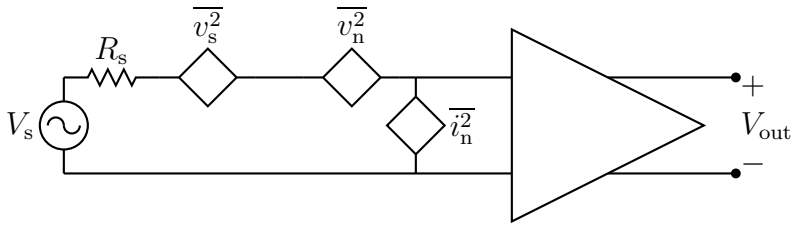

Figure 2.3: Noiseless amplifier with all noise combined into a voltage source, $\overline{v_n^2}$, and current source, $\overline{i_n^2}$.

2.4.4 Input Referred Noise of An Amplifier

In order to simplify noise calculations, all the noise of any amplifier can be modeled by two sources at the input of the amplifier, a voltage source, $\overline{v_n^2}$, and a parallel current source, $\overline{i_n}$, as shown in Figure 2.3 [29, p. 39]. The noise source $\overline{v_s}$ is from the source resistance. The equivalent noise voltage is calculated by shorting the input so that the source resistance is zero, and calculating the total noise. If the input is left open so that the source resistance is infinite, the resulting noise is the current noise. Using this procedure, the noise in any circuit can be represented by only two sources, as shown in Figure 2.3.

To find the noise referred to the input signal, all the noise sources can be referred back as described in [8]:

$$\begin{aligned}(\text{Total Noise})^2 = (\text{source resistor noise})^2 + (\text{voltage noise})^2 \\ +(\text{current noise} * \text{source resistor})^2\end{aligned} \tag{2.22}$$

which in this case becomes:

$$\overline{v_{tot}^2} = \overline{v_s^2} + \overline{v_n^2} + \overline{i_n^2}R_s^2 + C\overline{v_n i_n}R_s \tag{2.23}$$

The correlation C between these two sources is negligible in most practical circuits [12, p. 768]. The result $\overline{v_{tot}^2}$ represents the noise floor, which is the limit of the smallest signal that can be detected with that system.

2.4.5 Noise in Multiple Stages

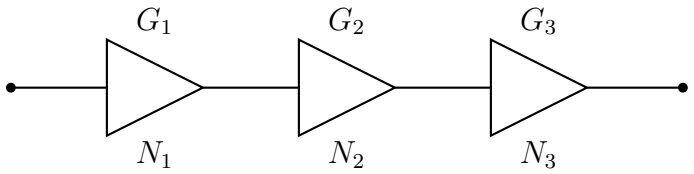

Figure 2.4: Amplifier with multiple stages, each with its own gain, G and noise power, N.

A multistage amplifier is shown in Figure 2.4. Each stage has a gain, G and contributes noise, N. The total output noise is easily calculated as

$$\begin{aligned} N_{\text{out}} &= (N_1 G_2 + N_2) G_3 + N_3 \\ &= N_1 G_2 G_3 + N_2 G_3 + N_3 \end{aligned} \tag{2.24}$$

Since the noise produced in the first stage is increased by the gains of all the subsequent stages, it is often the largest contributor to the total noise. Therefore, when designing a low noise circuit, minimizing the noise in the first stage is most important, while the noise in later stages can usually be neglected if the gains are large enough.

2.5 Transistor Models

The basic relationships of both bipolar and MOSFET transistors used in this work are reviewed below. These relationships provide the basis for the design calculations in Chapter 4. The noise properties of these devices are especially important in a low noise design, so the device noise models are also discussed.

2.5.1 Bipolar Transistor Characteristics

The collector current I_{C} of a bipolar transistor is exponentially related to the base-emitter voltage V_{BE},

$$I_{\text{C}} = I_{\text{S}} \exp\left(\frac{V_{\text{BE}}}{V_{\text{T}}}\right) \tag{2.25}$$

where V_{T}=kT/q, k is Boltzmann's constant (1.38 x 10^{-23} W-s/°K), T is the temperature in Kelvin, q is the charge of an electron (1.6 x 10^{-19} coulomb), and I_{S} is the saturation current. In all real BJT devices, the collector current also varies with the collector-emitter voltage V_{CE}. This dependence is called the Early effect, and modifies the above idealized expression to the following:

$$I_{\mathrm{C}} = I_{\mathrm{S}} \left(1 + \frac{V_{\mathrm{CE}}}{V_{\mathrm{A}}}\right) \exp\left(\frac{V_{\mathrm{BE}}}{V_{\mathrm{T}}}\right) \tag{2.26}$$

where V_{A} is the early voltage, and V_{CE} is the collector-emitter voltage.

The current gain of a bipolar device β is defined as the ratio of the collector and base currents:

$$I_{\mathrm{C}} = \beta I_{\mathrm{B}} \tag{2.27}$$

The base current, I_{B}, determines the current gain and depends on the process and layout properties of the specific device. Since β is not a constant, it is important to find a region that is relatively constant in order to improve the amplifier linearity. There is always some small recombination of carriers in the base region which becomes significant when the collector current is also small. This increase in base current decreases β. At very high currents, the collector current is limited by high-level injection and the Kirk effect, and again reduces β [12, pp 24 – 26].

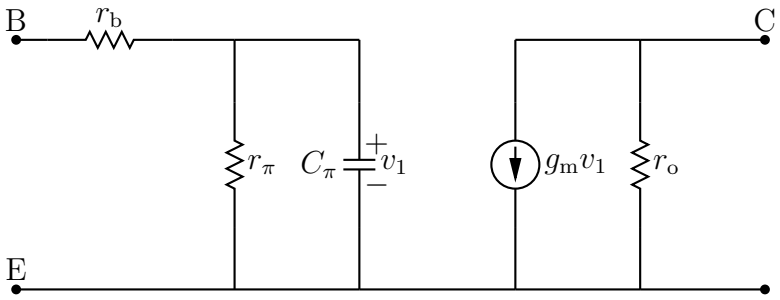

Figure 2.5: Small signal model of an NPN bipolar transistor.

A small signal model is used to clarify the gain relationships for the design process, and allows for noise and high frequency modelling. For small signals when the device is operating in the forward-active region, the transistor can be modeled as

shown in Figure 2.5. The emitter current is modeled as a dependent source which is proportional to the base-emitter voltage and the transconductance, g_{m}. The small signal transconductance depends only on the collector DC current:

$$g_{\mathrm{m}} = \frac{qI_{\mathrm{C}}}{kT} = \frac{I_{\mathrm{C}}}{V_{\mathrm{T}}} \tag{2.28}$$

The base-emitter resistance, r_{pi} is:

$$r_{\pi} = \frac{\beta}{g_{\mathrm{m}}} = \frac{\beta kT}{qI_{\mathrm{C}}} \tag{2.29}$$

This model will be used to represent the bipolar transistors in the design discussion in chapter 4.

2.5.2 Bipolar Transistor Noise Model

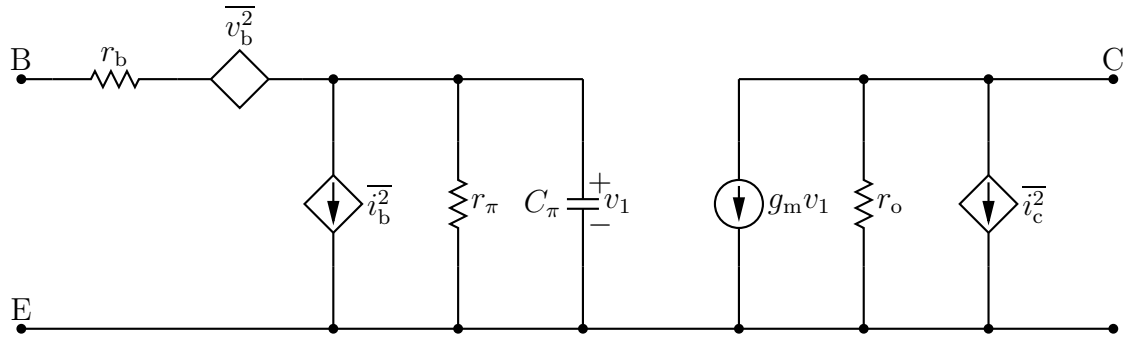

Figure 2.6: Noise model of an NPN bipolar transistor.

The small signal model discussed above can be expanded to include the noise sources. The noise model in Figure 2.6 shows the three largest noise sources, $\overline{v_{\mathrm{b}}^2}$, $\overline{i_{\mathrm{b}}^2}$, and $\overline{i_{\mathrm{c}}^2}$. These noise sources are a large part of the total amplifier noise, and so are described in more detail below.

The base voltage noise $\overline{v_{\mathrm{b}}^2}$ is from thermal noise in the base resistance, r_{b}.

$$\overline{v_{\mathrm{b}}^2} = 4kTr_{\mathrm{b}}\Delta f \tag{2.30}$$

The base resistance is between the base contact and the active region between the emitter and collector, so it can be minimized with careful layout technique. The base current noise $\overline{i_{\mathrm{b}}^2}$ is a combination of shot and flicker noise.

$$\overline{i_{\mathrm{b}}^2} = 2qI_{\mathrm{B}}\Delta f + K\frac{I_{\mathrm{B}}}{fA_{\mathrm{j}}}\Delta f \tag{2.31}$$

where A_{j} is the area of the base. The collector also has shot noise, resulting in the current noise $\overline{i_{\mathrm{c}}^2}$.

$$\overline{i_{\mathrm{c}}^2} = 2qI_{\mathrm{C}}\Delta f \tag{2.32}$$

2.5.3 MOSFET Transistor Characteristics

MOSFET devices are used in the second and third stages, as well as the bias circuitry. In an ideal MOSFET device operating in saturation, the drain current is quadratically related to the gate source voltage.

$$I_{\mathrm{D}} = \frac{\mu C_{\mathrm{ox}} W}{2L}\left(V_{\mathrm{GS}} - V_{\mathrm{th}}\right)^2 \tag{2.33}$$

However, because of channel length modulation, the drain current also depends on the drain-source voltage V_{DS}. To model this effect, the drain current equation is modified as follows:

$$I_{\mathrm{D}} = \frac{\mu C_{\mathrm{ox}} W}{2L}\left(V_{\mathrm{GS}} - V_{\mathrm{th}}\right)^2\left(1 + \lambda V_{\mathrm{DS}}\right) \tag{2.34}$$

where λ is the channel-length modulation coefficient and represents how much the channel varies compared to the fabricated length. The variation of the drain current (and therefore output impedance) of the transistor is a major source of nonlinearity when there is a large output voltage swing [38, pp. 25–27].

The small signal model is similar to the BJT and is shown in Figure 2.7. The transconductance is a measure of how the drain current changes with the gate-source voltage V_{GS}:

$$g_{\mathrm{m}} = \mu C_{\mathrm{ox}}\frac{W}{L}\left(V_{\mathrm{GS}} - V_{\mathrm{th}}\right) = \sqrt{2I_{\mathrm{D}}\mu C_{\mathrm{ox}}\frac{W}{L}} \tag{2.35}$$

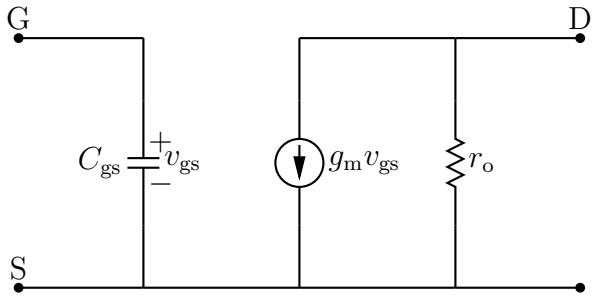

Figure 2.7: Small signal model of an NMOS transistor.

When channel length modulation is included, the transconductance becomes:

$$g_m = \mu C_{ox} \frac{W}{L} (V_{GS} - V_{th}) = \sqrt{2 I_D \mu C_{ox} \frac{W}{L} (1 + \lambda V_{DS})} \tag{2.36}$$

2.5.4 MOSFET Noise Model

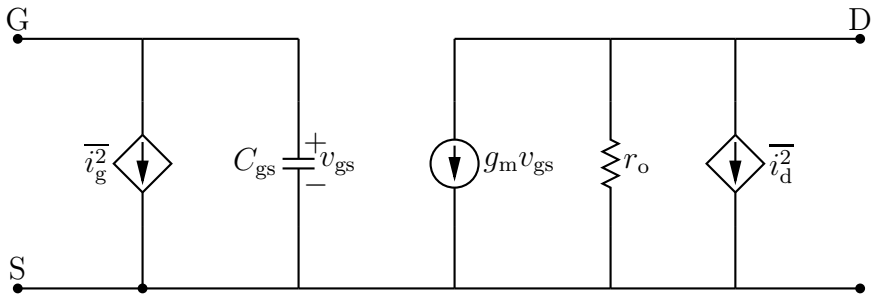

Figure 2.8: Noise model of an NMOS transistor.

MOSFETs have two main noise sources shown in Figure 2.8, $\overline{i_d^2}$ and $\overline{i_g^2}$. The drain current noise is a combination of thermal noise from the channel, and flicker noise.

$$\overline{i_d^2} = 4kT \frac{2}{3} g_m \Delta f + K \frac{I_D}{f A_j} \Delta f \tag{2.37}$$

The drain current noise represents the majority of the noise in a MOSFET. However, there is some small leakage of current across the gate, creating a gate current, I_G.

Since this gate current current is crossing an energy barrier, it has shot noise:

$$\overline{i_{\mathrm{g}}^2} = 2qI_{\mathrm{G}}\Delta f \tag{2.38}$$

At very high frequencies there is an additional component, which is generated by the thermal noise in the channel (and therefore correlated with the drain thermal noise). There are small changes in the local voltage produced as the charge carriers vibrate, which causes small capacitance changes, and results in an AC current through the gate. This current is in addition to the gate shot noise, and is frequency dependant [12, p. 759].

$$\overline{i_{\mathrm{g,high\,frequency}}^2} = 2qI_{\mathrm{G}}\Delta f + \frac{16}{15}kT\omega^2 C_{\mathrm{gs}}^2\Delta f \tag{2.39}$$

Chapter 3

Integrated Amplifier Challenges

The performance of the amplifier chip is critical to the success of the project as a whole. This chapter discusses the requirements and challenges to achieve the needed performance. The amplifier requirements, which drive every part of the design work, are presented first. Because of the unique combination of requirements, there are several special challenges for this design which are discussed next. Finally, an overview of previous work demonstrates that only a new, custom amplifier chip is capable of meeting the specifications.

3.1 Design Requirements

The specifications for the amplifier are derived from the requirements of the project as a whole. In order to minimize the physical size, the amplifier is integrated onto a chip using National Semiconductor's 0.25 μm BiCMOS process. This process has good low noise bipolar devices which are ideally suited for our application. As discussed in Section 2.2.1, the amplifier must have a low input impedance, because it improves the noise performance and keeps the receiver response flat in the chip bandwidth of 50 Hz–30 kHz. The amplifier's bandwidth easily extends beyond this specification on the high end, but $1/f$ noise presents the main challenge at the low frequencies.

The amplifier noise determines the sensitivity of the receiver, which determines the detectability of scientifically interesting signals. Therefore, the noise specification

is the most important and must be met even at the cost of other performance metrics. Given the antenna and transformer design described in Section 2.3, the 1 fT/$\sqrt{\text{Hz}}$ field noise specification for the project corresponds to a 7.8 pA/$\sqrt{\text{Hz}}$ input current noise. A gain for the chip of at least 15 mV/nA is required to ensure the signals are large enough to be accurately digitized. The chip should be linear enough to produce spurious free signals at the output swing of 1 V. All of these specifications must be achieved with only 5 mW of power that is budgeted for the amplifier.

3.2 Amplifier Design Challenges

The unusual combination of specifications of low input impedance, low operating frequency, low noise, and low power creates several special challenges for this design. These challenges, described below, are the main reasons for the lack of any amplifiers that satisfy the requirements, as discussed in the next Section (3.3).

3.2.1 Bipolar Transistors Required

In order to realize the 1 fT/$\sqrt{\text{Hz}}$ specification at low frequencies, low noise devices must be used in the first stage where the noise is most critical (see discussion 2.4.5). Although MOSFETs are the most common transistors used in integrated designs, their $1/f$ noise corners are in the megahertz range. The operating frequency range is for this amplifier is 4–5 orders of magnitude below the MOSFET's noise corner, resulting in $1/f$ noise that is prohibitively high.

The $1/f$ noise is large in MOSFETs because the gate field forces the channel current to flow very near the boundary to the oxide where the surface traps are, resulting in a very high rate of trapping. Alternatively, the current in bipolar transistors is more diffuse and flows in the bulk of the device away from the surface traps, resulting in much lower $1/f$ noise than MOSFETs. Also, bipolar devices have a larger number of carriers for the same current which also decreases the noise [49]. Because of the inherently much lower noise performance, bipolar transistors are ideally suited for this amplifier design.

Because bipolar devices are less popular, it has been increasingly difficult to find a process for their fabrication. Fortunately, the recent interest in bipolar devices for their superior performance at high frequencies (research in the gigahertz range), has made processes with bipolar devices available, making the implementation of this amplifier in an integrated circuit possible for the first time.

3.2.2 No PNP Transistors Available

Although the process used for the amplifier implementation has good low noise NPN bipolar transistors, it does not support PNP transistors. This practical limitation is because most bipolar transistors are being used for high frequency applications, and then only for the input device of the first stage. By using PMOS devices as the load in the first stage, a fully complementary process is not needed. As discussed above, the very large $1/f$ noise of MOSFETs at VLF frequencies prevents their use in the first stage at all. With only NPN transistors and resistors, the available topologies are severely restricted for low noise amplifiers.

It has been suggested that a PMOS in a Darlington connection with an NPN BJT creates a pseudo PNP device (see [48]). The overall equation for this composite device is then:

$$I_D = -(\beta_F + 1)\frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)(V_{GS} - V_t)^2 \tag{3.1}$$

from [12, p. 380]. However, this device suffers the same noise problems as using MOSFETs directly, so it can not be used in the signal path in the first stages.

3.2.3 Stages Must be DC Connected

In most amplifiers stages are connected through an AC coupling capacitor, which allows the signal to pass, but keeps the stages DC isolated. Each stage has its own bias network which keeps it from being affected by slight changes in the DC level of the previous stage. However, to do so at low frequencies in an integrated design, the coupling capacitors would have to be many times larger than the whole chip in order for the impedance to be small enough to not affect the signal. Therefore, all

the stages must be DC connected. In high gain amplifiers with DC coupling, even small changes in the DC level at the input can cause the whole amplifier to saturate, so the DC level of the signal path must be carefully controlled. Additionally, all the the biasing circuitry must be able to tolerate standard process and signal variations.

3.2.4 Headroom

The supply voltage in modern processes has been dropping as MOSFETs shrink in size. The National Semiconductor process used for our design has a maximum supply voltage of 2.5 V. The base-emitter voltage, V_{BE} must be around 0.7 V in order to be turned on (equivalently, MOSFETs need a similar gate-source voltage V_{GS} of 0.8 V). In order for the relationships described in Section 2.5 to be valid (i.e. the devices in the proper operating region) their collector-emitter voltage V_{CE} or drain-source voltage V_{DS} must be over around 0.6 V. Consequently, only three transistors can be stacked vertically between ground and the power supply with all of them biased properly. The limited transistor stack eliminates many common amplifier topologies, such as emitter degeneration and cascoding. This topology restriction chiefly affects the DC control and linearity performance.

3.3 Previous Work

Because of the unique combination of requirements for this amplifier, each design from the relevant published work meets only a few of the specifications. Most standard amplifiers are fabricated in CMOS technology now (see overview of examples in [42]), even for low frequency applications such as gravity research [2], so most bipolar examples are from the 1980s.

Optical sensors that use photodiodes require a low impedance current amplifier for detection. One example that is implemented in a discrete design [55] achieves 15.3 pA$\sqrt{\mathrm{Hz}}$ input referred noise, which is larger than the 7.8 pA/$\sqrt{\mathrm{Hz}}$. A more recent example has a 7.4 pA/$\sqrt{\mathrm{Hz}}$ noise floor but uses 65 mW of power [34]. However, optical sensors are designed for the gigahertz frequency range, and the sensor designs

are thus fundamentally different.

An audio range amplifier/instrumentation [8] uses complementary BJTs for good noise performance at low frequencies, however the common emitter topology for the input stage results in a high input impedance. The design achieves 3.5 nV/$\sqrt{\text{Hz}}$ voltage noise and 1.6 pA/$\sqrt{\text{Hz}}$ current noise at 10 Hz, but use 140 mW of power. Another BJT amplifier in the audio range achieves 1 nV/$\sqrt{\text{Hz}}$ to 3 nV/$\sqrt{\text{Hz}}$ at 10 kHz noise performance using a complementary BJT process [43]. But, with a high input impedance amplifier, and no power consumption listed, such a design would not work for our application.

Going further back in time when circuit integration was just starting to become widespread and PNP devices were still nonexistent or of poor quality, there are some designs in NPN only processes. One example is [3], which discusses various circuit designs for high impedance amplifiers and output stages. At that time the devices were physically larger, and the supply voltages were correspondingly higher as well, so that headroom was not a limiting factor. Often dual supplies were used for simpler biasing. Because of these reasons, these designs are fundamentally different and are unsuitable for our work. A very low power preamplifier [15] has a bandwidth from 0.02 Hz to 7.2 kHz with a power of 80 μW. The rms input-referred noise voltage is 2.2 μV/$\sqrt{\text{Hz}}$. However, it also has a large input impedance.

The work closest to the requirements of this project is an amplifier intended for SQUIDs, or Superconducting Quantum Interference Devices [26]. In this work, the source resistance ranges from 0.33 Ω to 1 Ω and the frequency range is 10 Hz to 100 kHz. The input referred noise voltage is 1.4 nV/$\sqrt{\text{Hz}}$ at 15 Hz and the current noise is 50 fA/$\sqrt{\text{Hz}}$ at 100 kHz. A transformer is used to step up the voltage from the sensor, however, a second transformer is used to provide feedback. Since these transformers are hand made, an extra one makes the cost of the preamplifier go up, as well as increasing the space required. This amplifier is not integrated and it uses FETs in a common source configuration. The power consumption is not give, but is likely to be quite high as it was not a design priority.

Some previous work use feedback to reduce the input impedance of a standard

Citation	Sensitivity	Source Impedance	Power
Erdi [8]	3.5 nV/$\sqrt{\text{Hz}}$	High	140 mW
Smith [43]	1 nV/$\sqrt{\text{Hz}}$	High	–
Harrison [15]	2.2 μV/$\sqrt{\text{Hz}}$	High	80 μW
Smith [43]	1.4 nV/$\sqrt{\text{Hz}}$	0.33 Ω – 1 Ω	–

Table 3.1: Summary of the most relevant published work in the VLF frequency range. Includes sensitivity, source impedance, and power consumption where available.

common emitter BJT when creating a current-to-voltage amplifier [37, 45, 31]. Another approach is to use feedback into the sensor itself as in [26] as discussed in Section 1.3.3. It is difficult to keep the amplifier stable for this topology with low input impedances, especially near 1 Ω. These awkward methods attempt to use a standard operational or instrumentation amplifier as a current amplifier, instead of designing a current amplifier directly to improve the noise performance. Therefore, in our work, the amplifier is designed specifically for a low input impedance.

A very early example of a current amplifier was intended for instrumentation [24]. However, with a large supply voltage, a large power budget, and no noise specification, such a design is not practical for our project. Some current amplifiers were used in nuclear research and the example [28] includes a common-base amplifier with that achieves a 0.98 nV/$\sqrt{\text{Hz}}$ voltage noise and 1.81 pA/$\sqrt{\text{Hz}}$. Since the amplifier bandwidth is in the Megahertz and Gigahertz range for nuclear research, and the power consumption is not a concern, these designs are also unsuitable for this work. Finally, some general common base amplifiers are collected in [5], but the designs are not optimized for noise or power.

Most of these designs satisfy only one or two of our requirements, and none of the designs satisfy all of them. A summary of the amplifiers designed for the VLF frequency range is shown in Table 3.1. Because no designs for this amplifier were already available, it was concluded that a new custom amplifier chip must be designed to overcome all of the special challenges listed above and meet the specifications.

Chapter 4

Amplifier Design

The custom amplifier requirements discussed in the previous chapter (Section 3.2) drive the design process. In each amplifier stage, the topology that can satisfy the requirements is chosen first. The various characteristics are calculated and used to adjust the design parameters for the best performance. The optimization of the noise of the first stage is presented in more detail since this method can be used for any amplifier using the same topology. Finally, the performance of the full amplifier is shown to meet the specifications.

4.1 Amplifier Overview

The amplifier has three stages as shown in the block diagram 4.1, and an DC feedback loop to regulate the DC levels. The first stage provides the low impedance match to the input, and coverts the signal to a high impedance output. Noise is the most important metric that drives the design choices for this stage. The second stage provides gain and level shifts the DC level for the correct biasing of the third stage, and the maintaince of the DC levels becomes the largest challenge. The last stage drives the output of the amplifier, and since it has the largest swing, linearity is most important. The design of each of the stage is discussed in subsequent Sections.

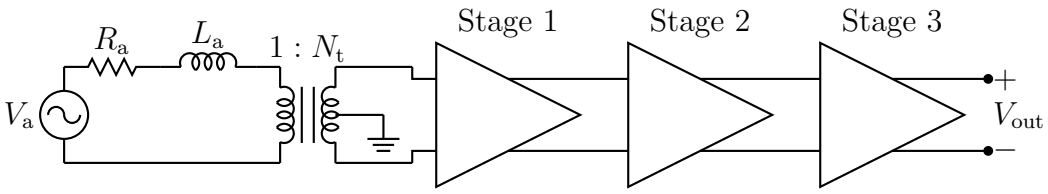

Figure 4.1: Block diagram of amplifier chip showing antenna, transformer, and three stages of the chip.

4.2 First Stage Topology and Design Relationships

4.2.1 Topology

The topology choice for the first stage is driven primarily by the low input impedance and noise specifications. The excessive $1/f$ noise in MOSFETs requires the use of bipolar devices as discussed in the special challenges Section 3.2. A common-base configuration provides the lowest input impedance and has been shown to result in lower noise [51]. Since PNP devices are not available, they can not be used as loads. The large $1/f$ noise of PMOS devices makes them unusable in the first stage as well, leaving resistors as the only viable load device. Although using resistors results in a lower gain due to their lower impedance, they do produce the best performance for low offset voltage and drift with temperature [8].

The first stage topology is shown in Figure 4.2, and includes the antenna and transformer. Because the center tap of the transformer is grounded, the DC level at the input is well controlled at a point physically close to the chip. The following Sections describe the equations governing the various parameters in this topology. All of the calculations and figures were done with the design parameters that were determined with the noise optimization as described in Section 4.3.

4.2.2 First Stage Input Impedance

The input impedance of the BJT in this configuration, including the resistance of the base, is ([12, p. 189]):

$$R_{\text{in}} = \frac{r_\pi + r_{\text{b}}}{1 + g_{\text{m}} r_\pi} \tag{4.1}$$

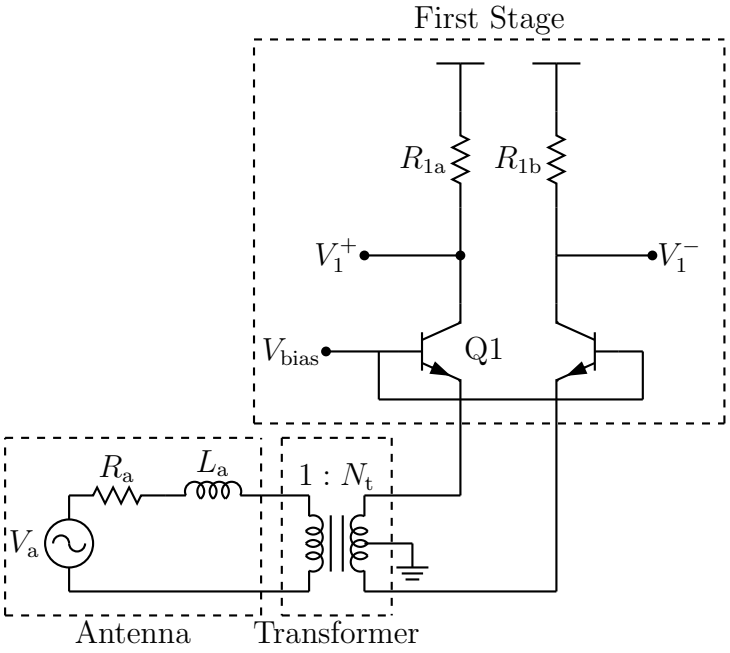

Figure 4.2: Topology of first stage, including antenna and transformer.

However, since $r_b \ll r_\pi$, the expression reduces to the following:

$$R_{in} = \frac{1}{g_m + \dfrac{1}{r_\pi}} \tag{4.2}$$

When the output resistance r_o is included (see small signal model in Section 2.5.1, the result is much more complicated:

$$R_{in} = \frac{1}{g_m + \dfrac{1}{r_\pi} - \dfrac{1}{r_o} - \left(\dfrac{g_m + \dfrac{1}{r_o}}{\dfrac{r_o}{R_L} + 1} \right)} \tag{4.3}$$

Because the output resistance r_o is large (483.6 kΩ), the difference between this full calculation and the previous simplified equation 4.2 is about 0.5%. Therefore the

simple expression 4.2 can be used for design work purposes, and simulations are used to confirm and fine tune the results. To find the total input impedance for the full differential first stage, the impedance must be doubled, so that the final expression used is:

$$R_{\text{in}} = \frac{2}{g_{\text{m}} + \dfrac{1}{r_\pi}} \tag{4.4}$$

4.2.3 First Stage Gain

The gain for a single NPN BJT in a common-base configuration, is

$$G_{\text{v}} = \frac{v_o}{v_{in}} = \frac{g_{\text{m}} R_{\text{L}}}{1 + g_{\text{m}} R_{\text{s}} + \dfrac{R_{\text{s}}}{r_\pi}} \tag{4.5}$$

If $R_{\text{s}}/r_\pi \ll g_{\text{m}} R_{\text{s}}$, which is true in this case, then the above simplifies to:

$$G_{\text{v}} = \frac{g_{\text{m}} R_{\text{L}}}{1 + g_{\text{m}} R_{\text{s}}} \tag{4.6}$$

If the base resistance is included, the expression becomes:

$$G_{\text{v}} = \frac{g_{\text{m}} R_{\text{L}}}{g_{\text{m}} R_{\text{s}} + \dfrac{R_{\text{s}}}{r_\pi} + \left(\dfrac{R_{\text{b}}}{r_\pi} + 1 \right)} \tag{4.7}$$

However, since $r_{\text{b}} \ll r_\pi$, this expression reduces back to equation 4.5. When r_{o} is included, the expression becomes:

$$G_{\text{v}} = \frac{g_{\text{m}} r_{\text{o}} + 1}{R_{\text{s}} \dfrac{r_{\text{o}}}{R_{\text{L}}} \left(\dfrac{1}{r_\pi} + g_{\text{m}} + \dfrac{1}{r_0} + \dfrac{1}{R_{\text{s}}} \right) + \dfrac{R_{\text{s}}}{r_\pi} + 1} \tag{4.8}$$

Again, the r_o is large enough in this case (483.6 kΩ), that it does not decrease the gain by much (about 0.4% in simulations). Therefore, equation 4.6 is used during design for estimating performance and evaluating tradeoffs, while the simulations use the full equation (4.8).

In this case where a differential signal is used, the gain is the same, as long as it is assumed that the reflected antenna impedance reflected across the transformer is halved ($R_s = Z_a/2$). It is important to note that since R_s changes with frequency, the gain of the first stage also changes with frequency. However, if the system as whole is considered with the antenna and transformer included, the frequency dependencies sum to a result that is flat in response over most of the bandwidth of interest (see equation 2.12 and following discussion).

Using the antenna and transistor parameters discussed in Section 2.3, the output voltage can be compared to the input current to find the amplifier current gain. If the antenna impedances are represented as $Z_p = j\omega L_p$ and $Z_c = j\omega C_s$, the Thevenin equivalent resistance and voltage source are:

$$R_{th} = \left[(Z_a \| Z_p)\, N_t^2 \right] \| \frac{1}{Z_c} \tag{4.9}$$

$$V_{th} = \left(\frac{R_{sec} + Z_p}{Z_a + R_{sec} + Z_p} \right) N_t^2 V_a \tag{4.10}$$

$$\text{where } R_{sec} = \frac{(Z_p \| R_{in})}{N_t^2}$$

The R_s in the above gain equations is one-half of this R_{th}. To find the output voltage compared to the input current, the input voltage is converted to the input current by multiplying the input impedance of the amplifier R_{in} (equation 4.2):

$$G_i = \frac{v_o}{i_{in}} = \frac{g_m R_L}{1 + g_m R_s + \dfrac{R_s}{r_\pi}\left(g_m + \dfrac{1}{r_\pi} \right)} \tag{4.11}$$

This current gain represents how much output voltage is produced with the given input current.

It is important to also calculate the performance of the front end of the system as a whole to ensure the amplifier will work properly. First the input signal is referred back to the antenna voltage V_a, resulting in the following gain :

$$\frac{v_\mathrm{o}}{V_\mathrm{a}} = G_\mathrm{v} N_\mathrm{t} \left(\frac{R_\mathrm{sec} + Z_\mathrm{p}}{R_\mathrm{sec} + Z_\mathrm{p} + Z_\mathrm{a}} \right) \tag{4.12}$$

To find how the output voltage relates to the input field, B, equation 2.5 is used with the above result to obtain the following.

$$\frac{v_\mathrm{o}}{B} = G_\mathrm{v} N_\mathrm{t} \left(\frac{R_\mathrm{sec} + Z_\mathrm{p}}{R_\mathrm{sec} + Z_\mathrm{p} + Z_\mathrm{a}} \right) (\omega N_\mathrm{a} A_\mathrm{a}) \tag{4.13}$$

To simplify the equations, the input angle is assumed to be zero for all of the design calculations.

4.2.4 First Stage Frequency Response

The high frequency 3 dB point of the transformer is determined by the parasitic capacitance between the windings, C_s. The pole formed from this capacitor and the input impedance of the amplifier is (from [35]):

$$f_\mathrm{c} = \frac{1}{2\pi C_\mathrm{s} R_\mathrm{in}} = 1.29\,\mathrm{MHz} \tag{4.14}$$

In this case the R_in is twice the input impedance of a signal common-base BJT (see Section 4.2.2).

The frequency response of the first stage is limited by the parasitic capacitances in the BJTs. The high frequency model is shown in Figure 4.3 (from [12, p. 514]), and includes two capacitors C_π and C_μ. The base-emitter capacitance C_π is a combination of the base-charging capacitance and the emitter-base depletion layer capacitance. The collector-base capacitance C_μ is from the junction capacitance between the collector and the substrate. The sizes of these capacitors varies directly with the device size,

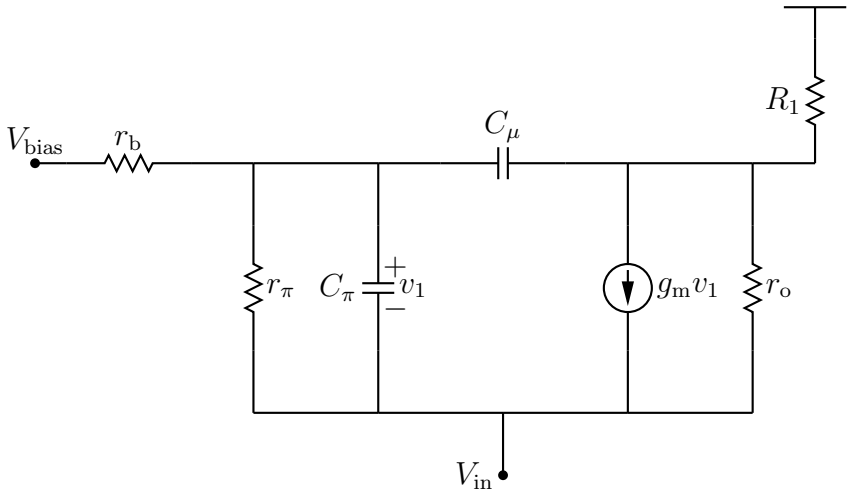

Figure 4.3: High frequency model of positive half of first stage, including NPN BJT and load resistor.

so as these devices are made larger to reduce $1/f$ noise, their capacitances increase as well. Solving for the transfer function results in the following:

$$\frac{v_{\text{o}}}{V_{\text{s}}} = \frac{g_{\text{m}} R_{\text{L}}}{R_{\text{s}}\left(1 + R_{\text{L}} C_\mu s\right)\left(\dfrac{1}{r_\pi} + g_{\text{m}} + \dfrac{1}{R_{\text{s}}} + C_\pi s\right)} \tag{4.15}$$

There are two poles, one associated with each capacitor. There is no Miller multiplication because there is no capacitance between the collector to the emitter [12, p. 515], so the poles are simply:

$$\begin{aligned} \text{Pole 1} &= \frac{1}{2\pi R_{\text{L}} C_\mu} \\ \text{Pole 2} &= \frac{\dfrac{1}{r_\pi} + g_{\text{m}} + \dfrac{1}{R_{\text{s}}}}{2\pi C_\pi} \end{aligned} \tag{4.16}$$

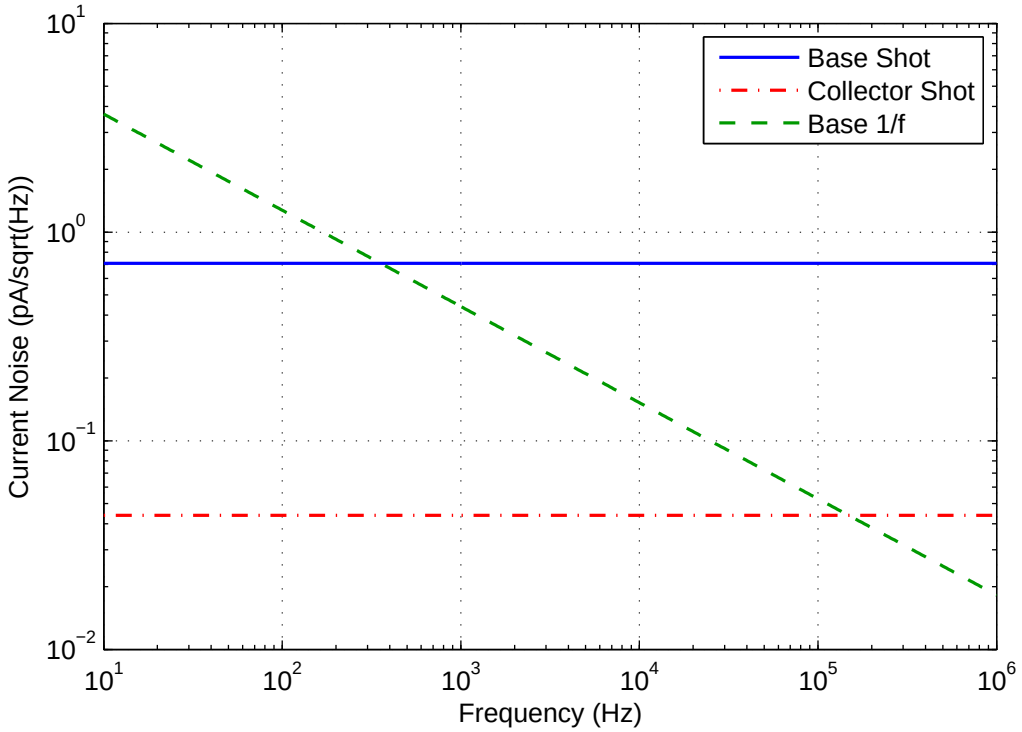

Figure 4.4: Comparison of noise sources in a NPN BJT in a common base configuration.

4.2.5 First Stage Noise

The noise sources in a bipolar transistor were discussed in Section 2.5.2. For comparison, these noise sources are plotted together in Figure 4.4. The base thermal noise can be reduced with careful layout technique to minimize the base resistance. In this design, the base thermal noise is six orders of magnitude less than any of the other sources, and therefore not visible on the graph. The base $1/f$ noise is dependant on the current density (see Section 2.4.3), so it can be reduced by increasing the size of the input transistors. Increasing these transistors also increases the parasitic capacitances (C_μ and C_π), which provide the limit to the bandwidth of this stage as discussed in the previous Section. Shot noise is left as the largest noise contributor in the transistors, and it is this noise that is optimized in Section 4.3.

As discussed in Section 2.4.4, all of the noise sources inside the transistor can be

represented by a voltage noise source and current noise source. For the common-base configuration, these equivalent noise sources are the same as for a common-emitter configuration [12, p. 783]. For the voltage noise, the two main sources are the thermal noise of the base resistance and the shot noise of the collector current.

$$\overline{v_{\mathrm{BJT}}^2} = \overline{v_{\mathrm{rb}}^2} + \left(\frac{\overline{i_c}}{g_{\mathrm{m}}}\right)^2 = 4kT\left(r_{\mathrm{b}} + \frac{1}{2g_{\mathrm{m}}}\right)\Delta f \tag{4.17}$$

The current noise is composed of the shot noise and $1/f$ noise of the base and the shot noise of the collector.

$$\overline{i_{\mathrm{BJT}}^2} = \overline{i_b^2} + \left(\frac{\overline{i_c}}{|\beta(jw)|}\right)^2 = 2q\left[I_{\mathrm{B}} + \frac{K_1}{2q}\frac{I_{\mathrm{B}}^a}{f} + \frac{I_{\mathrm{C}}}{|\beta(jw)|^2}\right]\Delta f \tag{4.18}$$

Using the equivalent noise sources from the BJT, a noise model for the whole first stage can be determined, as shown in Figure 4.5. The model includes the transistor noise along with the thermal noise of the load resistors.

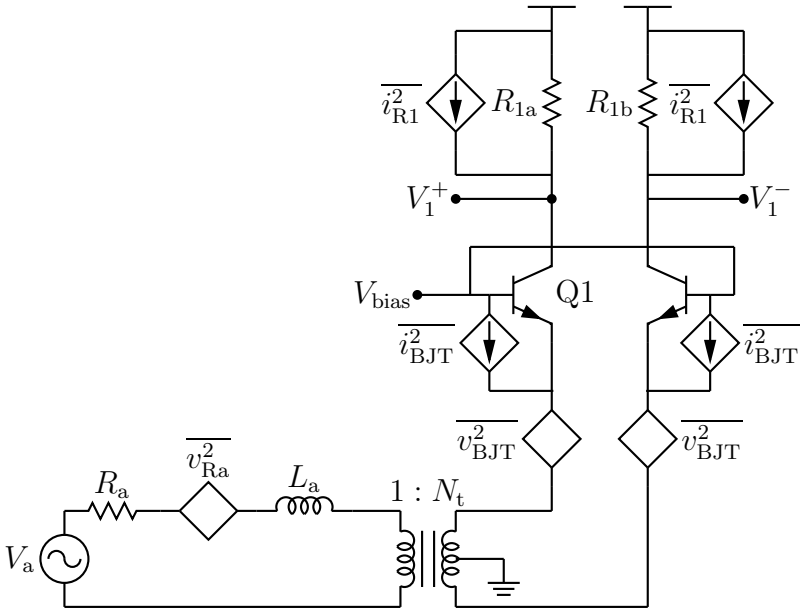

Figure 4.5: Noise model of the first stage and antenna. The transformer is assumed to be noiseless for design estimations, but the thermal noise in the parasistic resistances is included in simulation.

Because the current gain of a common-base BJT is unity, any current noise at the collector appears directly at the emitter unantennuated [12, page 783]. Therefore, the noise of the load resistors is more important than that for a usual common-emitter confinguration. These resistors also have a small amount of $1/f$ noise (see equation 2.21).

$$\overline{i_{RL}^2} = 4kT\frac{1}{R_{\mathrm{L}}}\Delta f + \frac{KI^{AF}}{wlf} \tag{4.19}$$

where w and l are the width and length of the resistor. For this process, if very large (20 μm) wide resistors are used, the $1/f$ noise is reduced below the other noise sources and becomes negligible.

The total current noise from the input stage, $\overline{i_{\mathrm{amp}}^2}$, can be estimated by combining all the noise sources at the input of the amplifier. When combining noise sources, the noise powers are added together, which requires that all of the noise currents to be summed in quadrature.

$$\overline{i_{amp}^2} = \overline{i_{\mathrm{BJT}}^2} + \overline{i_{RL}^2} + \frac{\overline{v_{\mathrm{BJT}}^2}}{R_{\mathrm{th}}^2/2} \tag{4.20}$$

$$\text{where } R_{\mathrm{th}} = \left[(Z_{\mathrm{a}} \| Z_{\mathrm{p}})N_a^2\right] \| \frac{1}{Z_{\mathrm{c}}} \tag{4.21}$$

All of the noise components are plotted together in Figure 4.6 for comparison. The load thermal noise is constant across frequency while the current noise has the expected increase at low frequencies from the $1/f$ noise. The large null in the voltage noise is an artifact of the resonance between the transformer inductance and parasitic capacitance. The BJT voltage noise is most important at the low and high ends of the bandwidth, while the thermal load resistor noise determines the noise in the midband. All of these sources vary differently with bias current as discussed in Section 4.3.

The noise sources from each side of the differential circuit must be added together as they are in series. The total noise can then be reflected back to the antenna using equation 2.14.

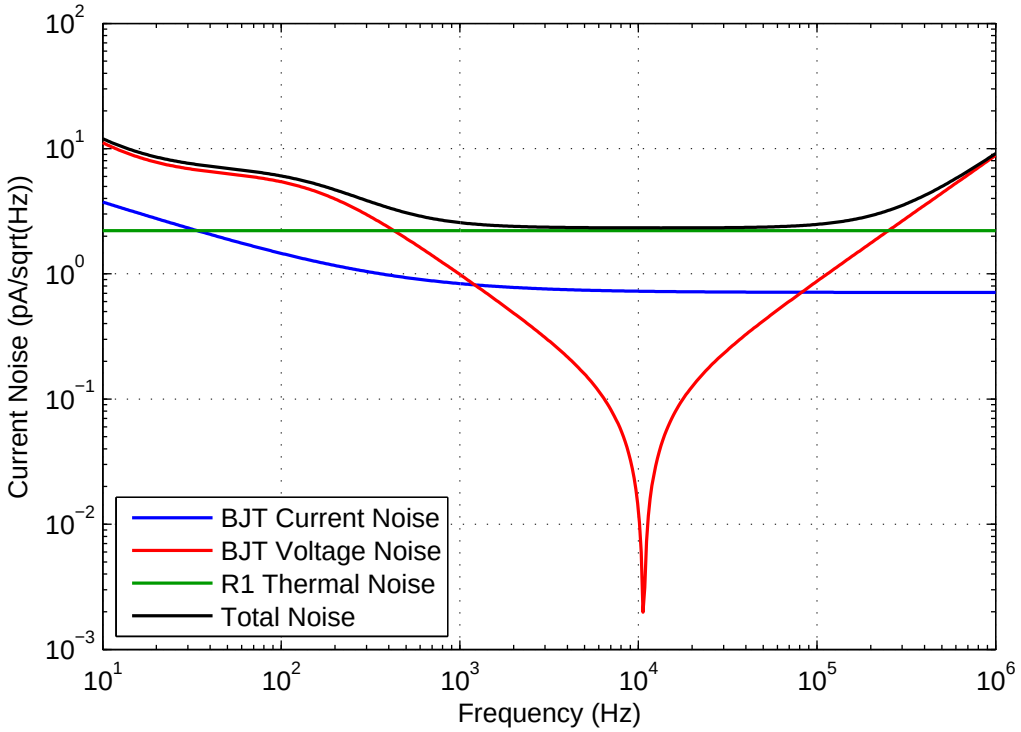

Figure 4.6: Comparison of all noise sources in the amplifier first stage, including the BJT voltage noise, BJT current noise, and load resistor thermal noise.

4.2.6 Temperature

Temperature has a large effect on BJTs because their operation depends on the carrier energy relative to the bandgap. Equation 2.25 shows that the collector current increases exponentially as the temperature decreases. However, the energy, and therefore concentration, of free electrons and holes decreases with temperature (I_S decreases) so that a larger V_{BE} is required to produce the same I_C. The early voltage is not affected as much because the various temperature effects cancel.

Simple simulations of the first stage can be done to find how these effects will alter the performance. The bias voltage is adjusted at both temperatures to maintain a DC current of 400 μA. When the temperature drops from 27 C to -50 C in simulation, the g_m increases by 34% , r_π increases by 37%, but the r_o does not change at all.

Therefore, the first stage will have a larger gain and, from equation 4.2, a decreased input resistance. Because the DC currents change so much with temperature, it is important to ensure the biasing circuitry can compensate for temperature variations. Current mirrors based on transistor ratios are used to the correct currents across the chip. The chip's resistors also experience changes in their characteristics. Since the diffusion resistors that used as a load in the first stage are based on charge carriers, they also change with temperature. The general equation for modelling the temperature change in a resistor is:

$$R(T) = R(T_{\text{nom}})[1 + TC1(T - T_{\text{nom}}) + TC2(T - T_{\text{nom}})^2] \tag{4.22}$$

The two temperature coefficients $TC1$ and $TC2$ are dependent on the fabrication process and are determined by empirical testing of devices in that particular process. Across the -50 C to 27 C temperature range, the resistors will only change by 8.9%, which is within the tolerance the circuit is designed to handle.

In addition to device characteristics, temperature also directly affect thermal noise (see equation 2.17). As the temperature drops in Antarctica, the thermal noise of the load resistor, antenna resistance, and any other parasitic resistance reduces as well. Therefore the noise performance will be better in the cold environment of Antarctica than normal room temperature. Shot noise is not affected at all, as long as the DC currents remain the same, and the $1/f$ noise is minimally affected [52].

4.3 Noise Optimization

In order to finish the design of the first stage, the sizes of the devices, bias current, and resistor values still must be determined. Noise is most important in this stage because it the largest contributor to the noise of the whole amplifier (see Section 2.4.5), so all of these parameters will be optimized for noise. The physical sizes of the resistor and transistors are made large enough to keep the $1/f$ noise below the shot and thermal noise sources. The remaining noise sources can be calculated in terms of the bias current I_{DC}, and then used to find the optimal current for the best noise

performance.

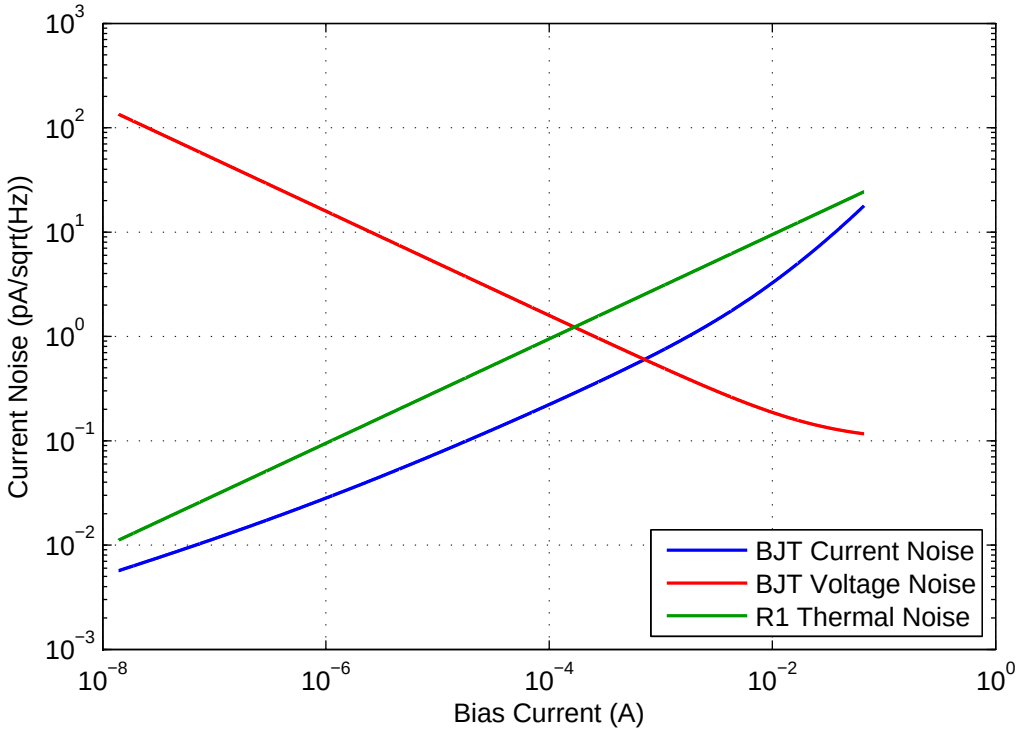

Figure 4.7: Noise components of first stage in terms of I_C at 1 kHz. The BJT voltage, BJT current, and load resistance noise sources are compared.

First, the load resistor R_1 generates thermal noise, as described in equation 2.17. In addition to providing the load to the transistors, the resistor R_1 also sets the DC level of the input of the second stage. The size of the resistor should be maximized for the largest gain and the smallest thermal current noise, so the output DC level should be set at the minimum the second stage can accept. In this case, the output level is set to 1.1 V, so there is a 1.4 V drop across the resistor. The resistor value in terms of I_C is:

$$R_L = \frac{V_{drop}}{I_C} = \frac{1.4\text{V}}{I_C} \tag{4.23}$$

By using the above equation 4.23 for the load resistor noise and the β vs I_C curve for the transistor with equation 4.20, all of the noise sources are in terms of the bias

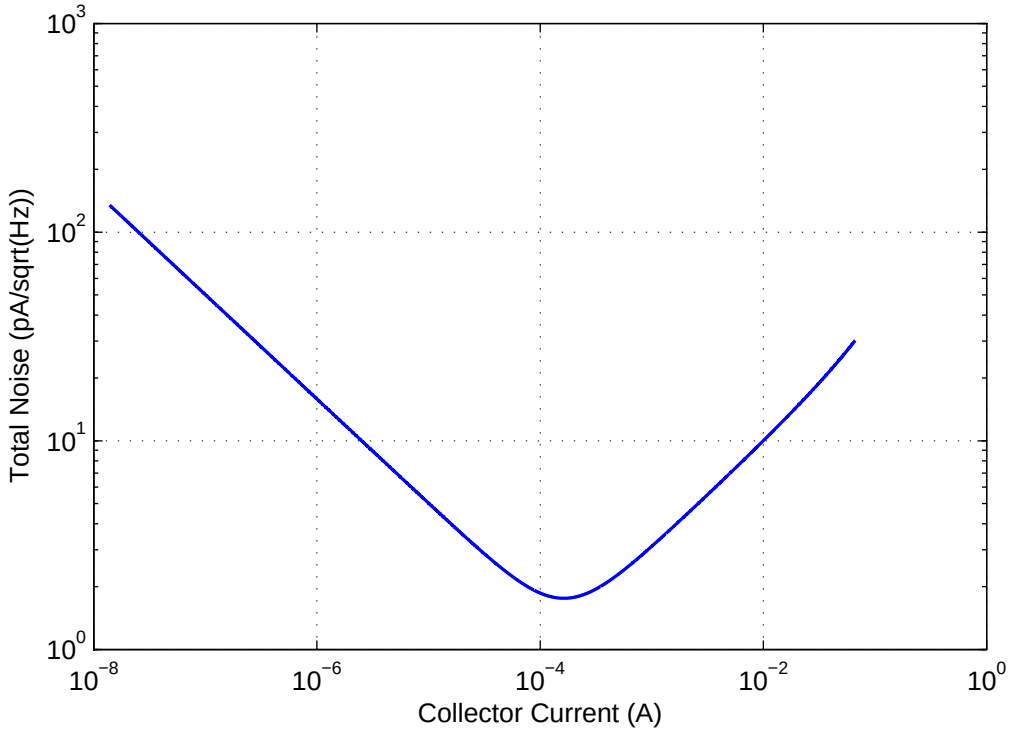

Figure 4.8: Total noise current of first stage at 1 kHz, showing minimum at 163 μA.

current I_C. The result is plotted in Figure 4.7. The current and resistor noise increase with bias current, while the voltage noise decreases. When these sources are added together to calculate the total noise, there is a clear minimum (see Figure 4.8). This minimum at 163 μA, represents the bias current that produces the lowest noise at 1 kHz.

Using this method for several different frequencies and plotting the results together produces Figure 4.9. The noise minima occur at lower bias currents over most of the bandwidth. Because the amplifier must work over a wide bandwidth of frequencies and only one bias current can be chosen, there must be a compromise. At lower bias points, the noise varies greatly with frequency (the curves are all separated), but at higher bias currents, especially above 1 mA, the noise is much more constant (the curves are nearly on top of each other). Therefore, choosing a larger bias current

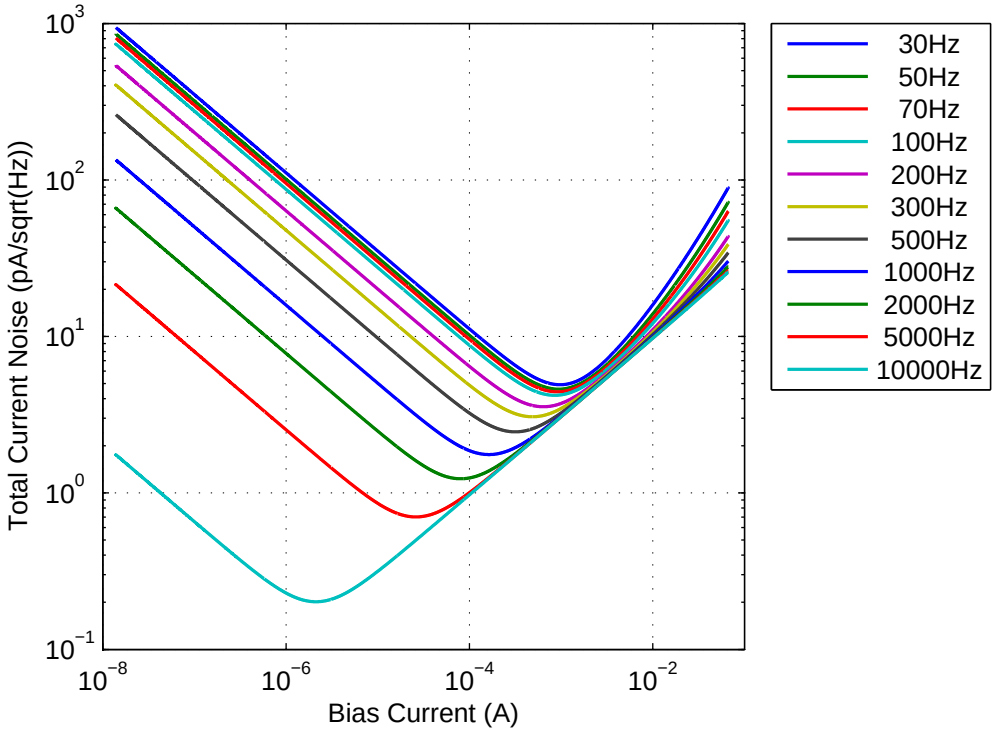

Figure 4.9: Total noise current of the first stage at various frequencies. The minimum at each frequency occurs at a lower bias point as the frequency increases.

produces in a more constant (or flatter) noise floor.

By plotting all of the bias currents at the minimum noise for each frequency as shown in Figure 4.10, it is easier to see the dependence on frequency. When choosing the bias point, it is also important to consider the 5 mW power limit. At a 2.5 V supply, only 2 mA of current is available for the whole amplifier. Additionally, a larger current results in a larger load resistor, which produces more gain. For this design, a bias of 400 μA results in good performance at low frequencies, keeps the noise response flat in the middle of the band, and leaves 1.2 mA available for the rest of the amplifier.

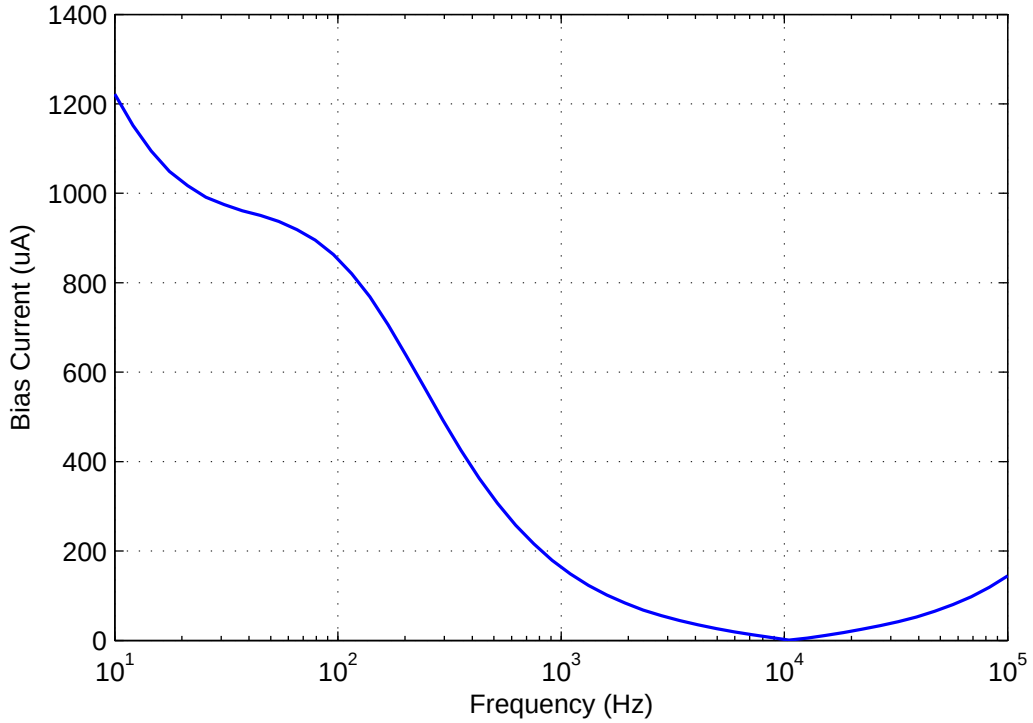

Figure 4.10: Bias current for minimum noise across frequency. For most of the band of interest the minimum noise current decreases with frequency. A single bias point must be chosen for the amplifier, requiring a compromise.

4.4 First Stage Final Design

The selection of the bias current determines the remaining design parameters. The load resistors R_{1a} and R_{1b} are set to 3.5 kΩ to ensure the correct output voltage of 1.1 V. Since these resistors can change by 10% during fabrication, the output voltage will stay above 1 V over the process variations.

The first stage voltage gain is calculated to be 10.9 at DC, from equation 4.6. Since this gain is dependant on the load resistors directly, the gain will vary by the same 10% that the resistors do. The bandwidth of the gain is limited by the parasitic capacitances of the input transistors Q1. With C_μ = 514 fF, the first pole is at 88.5 MHz, far above the needed frequency range (see equation 4.16. The other pole

changes with R_s and therefore is more complicated. When the $C_\pi = 3.88$ pF is used and the pole calculated across the frequency range, the pole settles to about 637 MHz. Since these poles are out of the band of interest, this stage does not limit the amplifier bandwidth.

The input impedance described in equation 4.4, with the 400 μA current results in 128.2 Ω. When this input impedance is reflected across the transformer, the result is a 0.501 Ω input impedance at DC. Since the impedance is lower than needed, the parasitic resistances of the transformer, bond wires, and connectors can be accommodated.

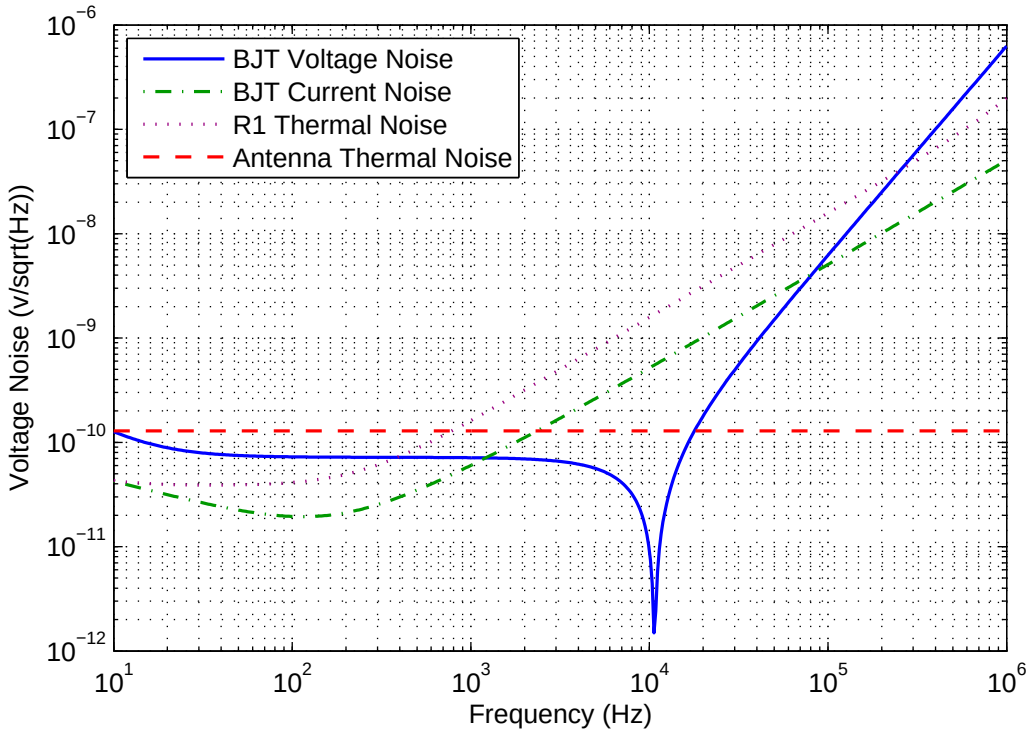

Figure 4.11: Amplifier and antenna noise referred to antenna input.

The total noise reflected back to the antenna is plotted in Figure 4.11. Below 1 kHz, the amplifier noise drops below the antenna noise. At the lower band, the noise performance of the system is limited only by the thermal resistance of the antenna.

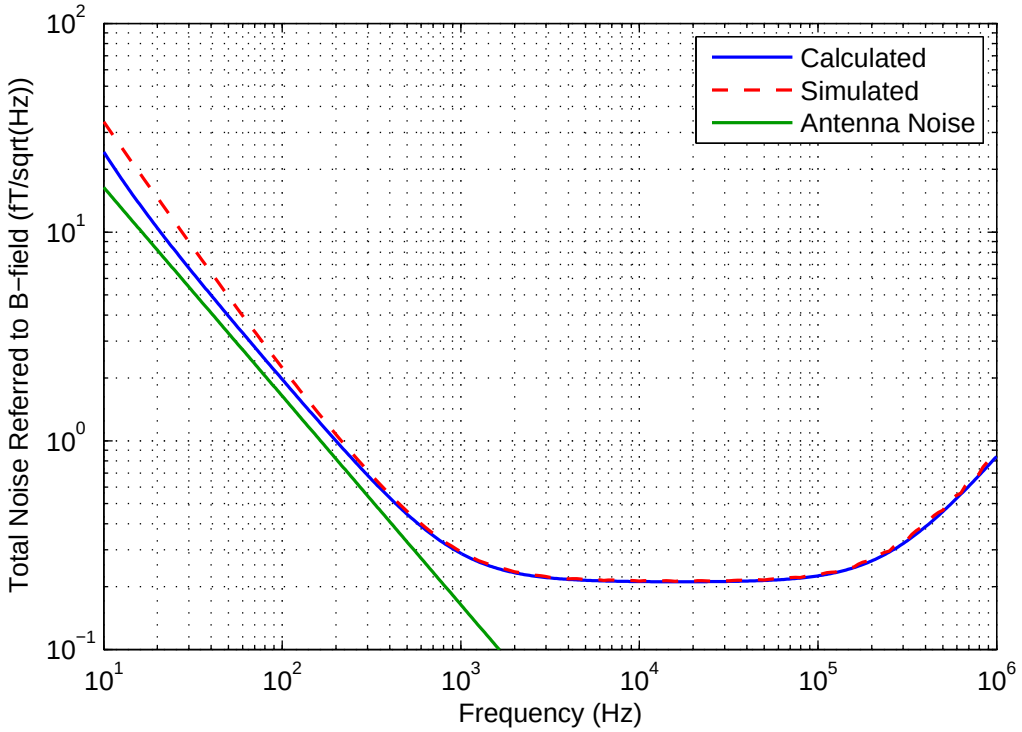

Figure 4.12: Amplifier and antenna noise referred to equivalent magnetic field. A triangular antenna with a 10m base and 5 turns was used.

By incorporating the antenna parameters that are used in the final system, the noise can be referred back to the magnetic field as in equation 2.15. The 10 m base, 5 turn triangular antenna is used to calculate the field noise shown in blue Figure 4.12. It is clear that the frequency dependence of the induced voltage in the antenna, V_{a}, and the reactance of the transformer together produce a response that is flat over two frequency decades, just as discussed in Section 2.2.1. The antenna thermal noise (included in total noise calculation) is also depicted separately in green to indicate the fundamental sensitivity limit for the system. The simulated curve matches the calculations closely, which confirms that the calculations described in the Topology Section above (4.2.1) approximate the performance well and that all of the major contributors are accounted for and modeled properly. The total noise stays below the 1 fT/$\sqrt{\mathrm{Hz}}$ specification above 200 Hz, which means the small electronmagnetic

signals will be visible with this amplifier.

4.5 Second Stage

The second stage provides gain for the amplifier, while maintaining the correct DC level to bias the output stage properly. The output DC level of the first stage changes directly with the load resistor values. Since the process tolerances for these resistors are at about 10% this stage should be able to handle a 10% variation in input DC levels. It must also have a high input impedance in order to minimize the loading on the sensitive first stage. Since the current gain of the first stage is unity, all of the current noise at the input of the second stage is just as important as the first stage. For this reason, BJTs are used instead of MOSFETs for the second stage as well as the first stage.

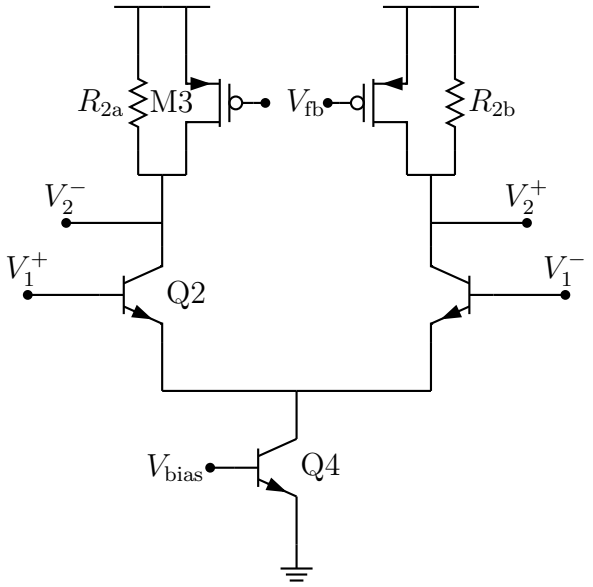

Figure 4.13: Topology of Second Stage.

A standard differential pair was chosen for the topology, which is shown in Figure 4.13. This topology rejects common mode signals and therefore accommodates large changes in input DC levels. The tail current is generated by a BJT in order to

provide good temperature compensation and coordination with the first stage. Since the loads of this device are not connected directly to the first stage, MOSFETs can be used, allowing for tighter control of the output DC level. The resistors provide some temperature compensation as well as reducing the gain to improve stability. The three stages of gain provide ample gain for this application, so it not important to maximize it. The load resistors set the DC level with the PMOS devices (M3) fine tuning it. Since this is a high gain stage, small capacitors are required between the output and input to compensate the stage and remove any tendency torward unwanted oscillations above the band of interest.

4.5.1 Second Stage Gain

The gain of a differential pair is the transistor transconductance multiplied by the output impedance. Since the impedance of the load resistor is much lower than the parallel combination of the NPN and PMOS transistor, it is the only one included in the gain equation.

$$G_2 = g_{\mathrm{m}} R_{\mathrm{L2}} = \frac{I_{\mathrm{C}} R_{\mathrm{L2}}}{V_{\mathrm{t}}} \tag{4.24}$$

4.5.2 Second Stage Frequency Response

Since the band of interest is below 100 kHz, a Miller capacitor C_{m} is used between the output and input of the stage to limit the bandwidth of the stage and the potential for unwanted oscillations. This capacitor increases the feedback capacitance well beyond the C_{CB} parasitic capacitance and pushes the pole lower in frequency. The apparent capacitance is increased by the gain of the first stage, so a relatively small Miller capacitance can have a large effect on the pole. The equation for the pole location is as follows:

$$\mathrm{Second\,Stage\,Input\,Pole} = \frac{1}{2\pi R_{\mathrm{L1}} C_{\mathrm{m}} (1 + G_2)} \tag{4.25}$$

This pole determines the gain rolloff frequency for this stage, so the Miller capacitor should be chosen to set the bandwidth as needed.

4.5.3 Second Stage Noise

The stage has noise contributions from the BJT devices, load resistors R_2, and load PMOS devices. The BJT current and voltage noise is the same as in the common base configuration (equations 4.17 and 4.18). The resistor load has thermal noise just like the first stage:

$$\overline{i_{R2}^2} = 4kT\frac{1}{R_2}\Delta f + \frac{KI^{AF}}{wlf} \tag{4.26}$$

The PMOS devices produce shot and $1/f$ noise as discussed in Section 2.5.4. When all of the noise sources of the PMOS device are represented by two sources (2.4.4), in the same manner as with the BJT devices, the sources are:

$$\overline{v_{\mathrm{PMOS}}^2} = \frac{\overline{i_d^2}}{g_{\mathrm{m}}^2} = 4kT\frac{2}{3}\frac{1}{g_{\mathrm{m}}}\Delta f + K\frac{I_{\mathrm{D}}}{g_{\mathrm{m}}^2 f A_{\mathrm{j}}}\Delta f \tag{4.27}$$

$$\overline{i_{\mathrm{PMOS}}^2} = \overline{i_g^2} + \frac{\omega^2 C_{\mathrm{gs}}^2}{g_{\mathrm{m}}^2}\overline{i_d^2} = 2qI_{\mathrm{G}}\Delta f + \frac{\omega^2 C_{\mathrm{gs}}^2}{g_{\mathrm{m}}^2}\left(4kT\frac{2}{3}g_{\mathrm{m}} + K\frac{I_{\mathrm{D}}}{fA_{\mathrm{j}}}\right)\Delta f \tag{4.28}$$

The PMOS noise is greatly reduced because it must be divided by the gain of the second stage in order to refer it back to the input.

A noise optimization could be done with this stage just like the first stage. However, as long as the noise from this stage stays below the first stage noise, it does not matter whether the noise in the second stage is reduced to the optimal level. Instead, it is best to conserve bias current in order to meet the power specification, once the noise is reduced until it no longer affects the amplifier as a whole.

4.5.4 Second Stage Design

With a tail current in device Q4 of 345 μA and a load resistor R_2 of 8 kΩ, the second stage has a gain of 58.1. The gain rolls off at 30.7 MHz, well above the needed bandwidth.

All of the noise sources from the second stage are compared together, along with the first stage in Figure 4.14. By making the bipolar devices in the second stage large enough, the noise they contribute remains below the current noise from the first stage across the full bandwidth. Since the PMOS noise is several orders of magnitude larger

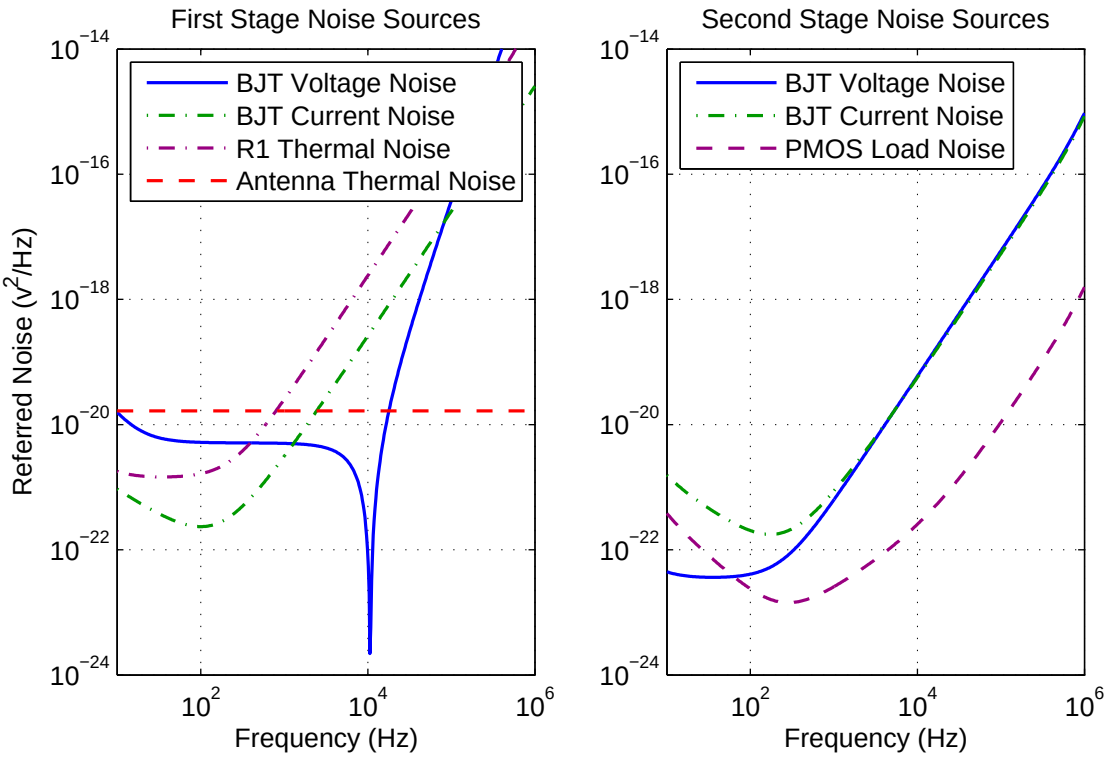

Figure 4.14: Comparison of noise components for the first two stages and the thermal antenna noise, referred back to the antenna. The first stage includes the BJT voltage noise, BJT current noise, and thermal noise from R_1. The second stage also includes the BJT voltage noise, BJT current noise, and an a PMOS load.

than the thermal noise from the resistor loads R_2, the resistor noise is not shown. It is clear that the total noise contributed by the second stage is lower than the first stage, and therefore this stage does not affect the noise performance of the amplifier as a whole.

Figure 4.15 shows the total noise referred to the field. This result is nearly identical to Figure 4.12, which again shows that the second stage design does not degrade the sensitivity of the amplifier.

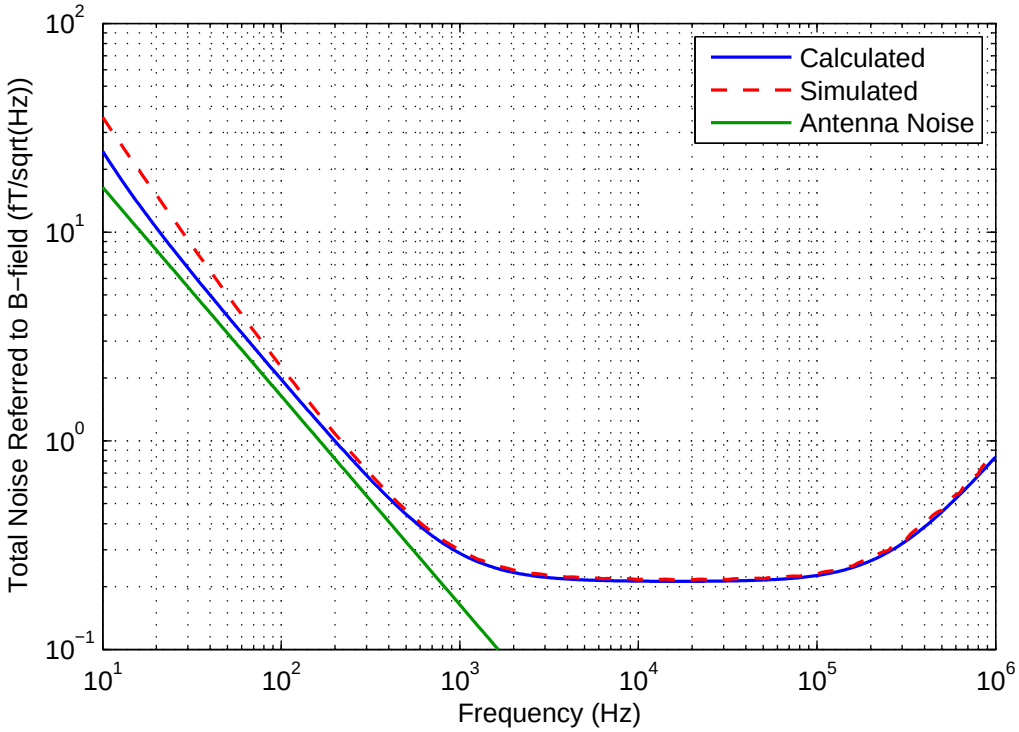

Figure 4.15: Total noise from the first two stages referred back to the input field. Assumes a 10 m base triangular antenna with 5 turns.

4.6 Output Stage

The main purpose of the output stage is to provide enough current for the entire voltage swing of 1 Vpp to be as linear as possible. The output voltage also needs to remain as close to the half of the supply voltage (1.25 V) as possible to accommodate the swing. This amplifier is not an Op-Amp, so the amount of current it needs to supply is not large. An aggressive specification for this amplifier would be to drive a 100 pF capacitor at 50 kHz. In this case only 31 μA is needed, and so a quiescent current of 285 μA would be plenty to slew sufficiently. This 285 μA current represents only 15% of the entire power budget and so it will keep the amplifier below the power budget.

Since there is not enough headroom for emitter degeneration, the topology for the

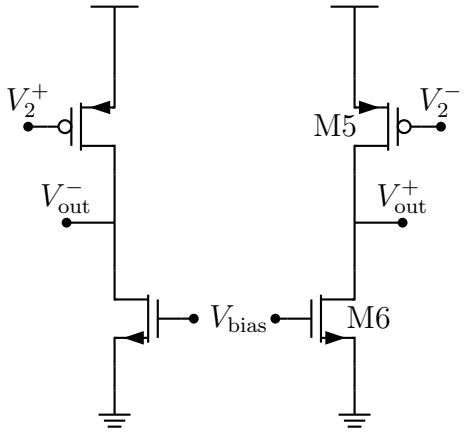

Figure 4.16: Topology of third stage.

output stage is a simple common-emitter amplifier with an active load, see Figure 4.16. Using a PMOS device in the signal path is unusual, but at these low frequencies, the device speed is not an issue, and the gain reduction is easily made up by the other two stages. Additionally, an extra level shifting step is not required because the output DC level of the second stage is already high.

4.6.1 Third Stage Gain

Since this stage has a standard topology, the gain calculation is straightforward.

$$G_3 = g_{\text{m}} R_{\text{o}} = 211 \tag{4.29}$$

The output resistance R_{o} is a combination of the output resistance of the PMOS device (Q5) and the load (Q6). This topology does assume a high impedance load, since the load will be in parallel with the output resistance, and cause a reduction in gain.

The bandwidth of this stage is limited only by the parasitic capacitances of Q5. Both MOSFETs in this stage are made large in order to improve linearity and matching, however the parasitic capacitances are also increased which then limit the bandwidth. Because of Miller multiplication, the main pole is determined by the gate-drain

capacitance

$$\text{Pole} = \frac{1}{2\pi R_o C_{GD}(1+G_3)} = 5.53\,\text{MHz} \tag{4.30}$$

Because this pole is well outside of the band of interest, it does not affect the amplifier as a whole, but removes any unexpected oscillations at high frequencies.

4.6.2 Third Stage Linearity

Linearity determines the quality (or fidelity) of the received data, and is required for confidence in the recorded data and scientific results. Although MOSFETs are generally assumed to be linear in normal operating conditions, they follow a square law relationship (see equation 2.33). This nonlinearity is the most apparent when the signal has a large swing, and so is most important in the output stage. Linearity is often improved with topologies that linearize the transistors, such as emitter degeneration and cascoding. However, these topologies are not possible with such a low supply voltage.

The design parameters must then be optimized for linearity within the limited topology. Because the amplifier is fully differential, all of the even harmonics are cancelled out, leaving only the third and fifth harmonics as major contributors. Channel-length modulation causes the output impedance to change with the drain-source voltage as discussed in Section 2.5.3. However, in short channel devices, the drain induced barrier lowering has the opposite effect, resulting in a more linear response [38, p. 591].

Another mitigating effect is velocity saturation, which occurs in modern devices with short lengths. Velocity saturation linearlizes the relationship of I_D to V_{GS} and also minimizes the effects of pinch off in the channel, reducing the effects of a changing V_{DS} [38, pp. 587–589]. Therefore, linearity is also improved by increasing V_{DS}, or lowering the output DC level. Since the mobility of PMOS devices is lower than an NMOS, they reach this condition much quicker, which means that PMOS devices are actually more linear than NMOS and is another reason they were used in the signal path in this stage.

4.7 DC Level Control

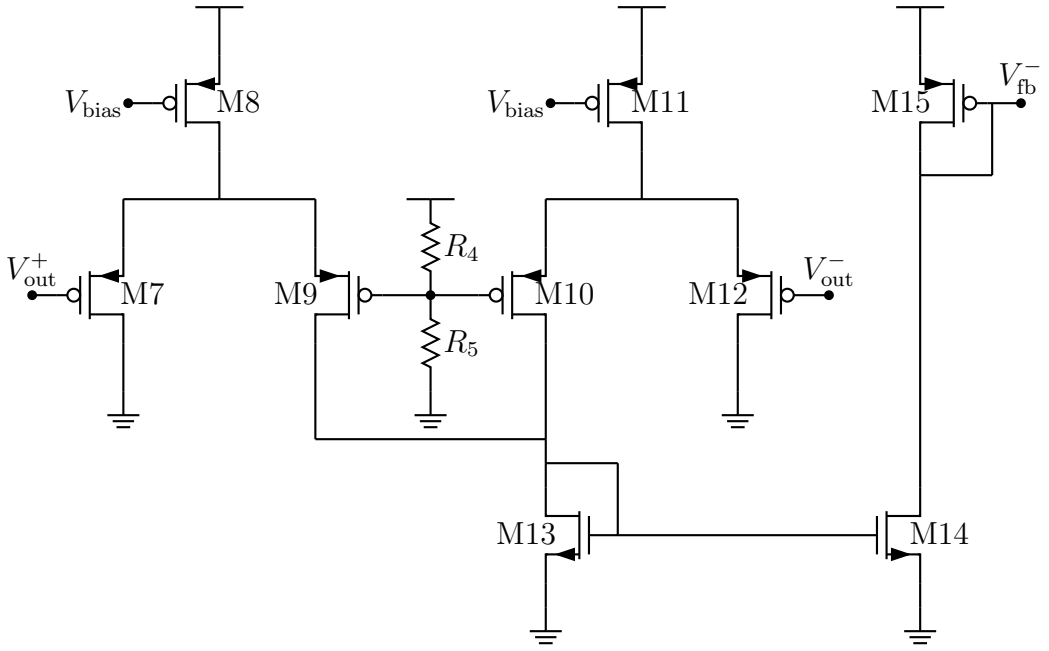

Figure 4.17: Schematic of feedback for DC control. The generated voltage V_{fb} is used to bias the load MOSFETs M3 in the second stage.

The output DC level must be kept near 1.25 V to allow for a large output swing. The second stage easily accommodates large changes from the first stage, so only the second and output stages must be controlled. The output voltage is maintained by small feedback circuit which compares the output voltages with a standard voltage developed by a resistor divider (R_4 and R_5). Since the matching between devices in integrated circuits can be less than 1% with careful layout, the resistor divider will produce the correct reference voltage, even if the absolute value of the resistances varies with the process. The difference in the output voltages are added together (M13) and then fed back (with M15) to the load PMOS devices M3 in the second stage. Since this circuit is out of the signal path and in the back end of the amplifier, it does not affect the noise at all. The sensing transistors M7 and M12 must be as small as possible to minimize the loading on the output transistors and preserve the linearity.

4.8 Full Amplifier

Combining all of the stages together results in the final amplifier design that must be characterized as a whole. It is important to make sure that the stages do not cause unexpected interferences, so the simulated performance of the full amplifier is compared with the specifications.

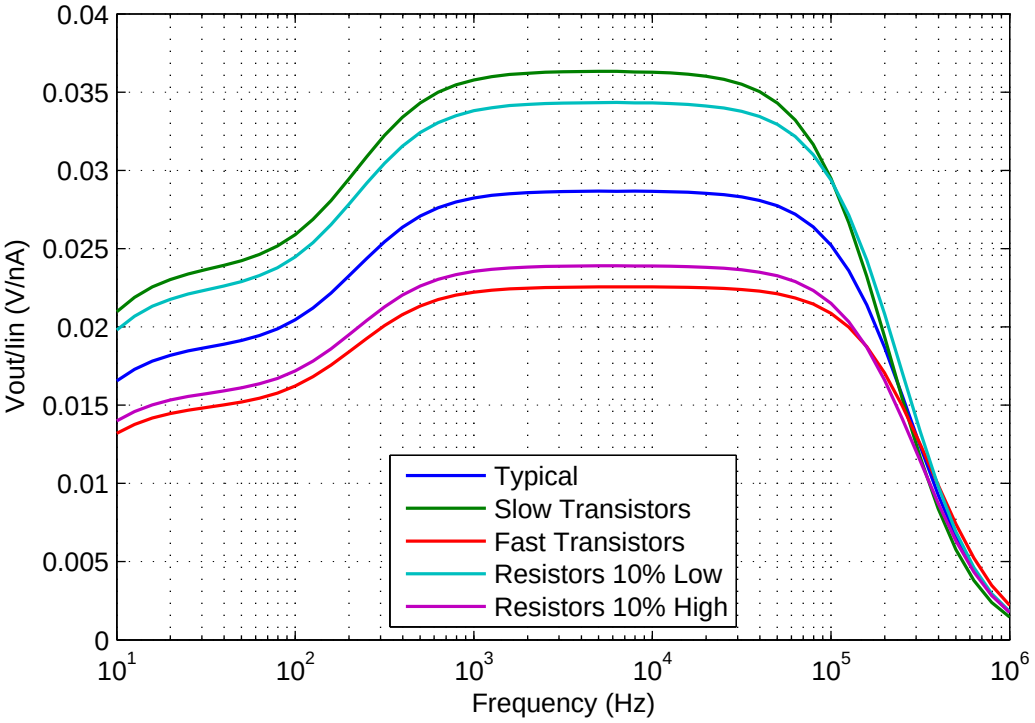

Figure 4.18: Total current gain of the full amplifier. Several process variations are shown, including the resistors changing by 10% and the transistor properties.

The total gain is shown in Figure 4.18 in blue. Although the gain appears to rolloff at low frequencies, the gain is actually flat to DC. This rolloff artifact of the simulation method for the transformer. In order to make sure the chip will still function well over process variations, several example cases are graphed. In this case the "slow" and "fast" transistor models represent the extremes of the process variations alterations to the device performance. Although the gain changes with

these variations, the amplifier still works and keeps the same frequency response. The resistors were also varied by 10%, and again, the gain magnitude changes, but the circuit works as expected. Throughout all of these variations, the gain exceeds the 0.015 V/nA specification.

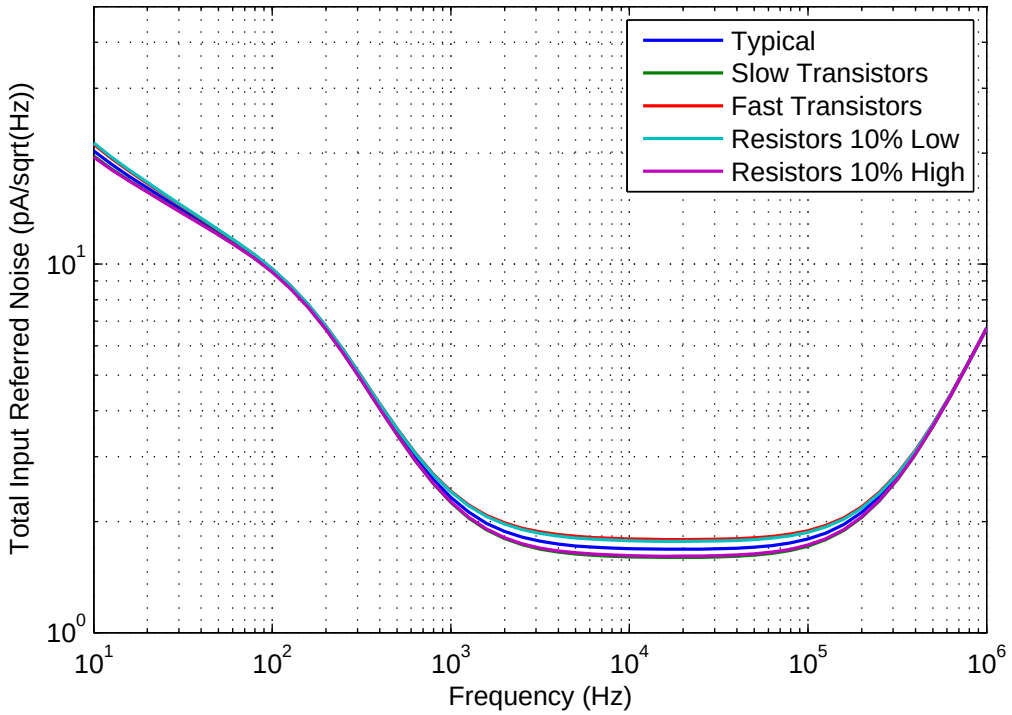

Figure 4.19: Total current noise of the full amplifier. Several process variations are shown, including the resistors changing by 20% and the transistor properties.

The total noise is graphed in Figure 4.19 and remains essentially the same as the first stage noise shown in Figure 4.6. The minimum is at 1.8 pA/$\sqrt{\text{Hz}}$, and stays below the 7.8 pA/$\sqrt{\text{Hz}}$ down to 130 Hz.

The input impedance is 0.501 Ω which is a good match the input signal. The linearity is the performance metric that was not met, due to the low supply voltage. Without enough headroom for stacking the linearity suffered. Although it would be ideal to design for the full 96 dB dynamic range of the ADC, only 68 dB was achieved. The amplifier's power consumption was kept below the 5 mW limit at only 4.63 mW

of power.

4.9 Layout

Layout for analog designs, and especially for low noise designs, must be done by hand instead of using automatic algorithms because careful attention must be paid to ensure the parasitic resistances and capacitances do not impact the amplifier performance, especially noise [22]. Every metal line and via between layers adds resistance, thus wide lines and multiple vias must be used in critical areas. In this design the resistance in the two input signal lines are most crucial and can degrade the noise performance of the whole amplifier. All of the parasitic resistances should be reduced below the antenna resistance of $1\,\Omega$. The base resistance must also be minimized as discussed in Section 4.2.5.

In a differential design, a small mismatch between the two signal paths is amplified and can cause the output voltage to rail to either ground or power, rendering the amplifier useless. It is important to ensure that all of the devices in the two paths are as identical as possible so that their characteristics are matched to prevent the DC saturation. Since there are variations across a wafer that occur during fabrication, the best way of improving matching is by using a common-centroid layout [12, p. 476]. Each transistor, resistor, and capacitor in the design is split into several smaller devices, and then arranged in a common-centroid pattern. Unfortunately, this technique often makes the metal connections between the devices more complicated, so it is important to ensure that the resistances from the extra vias are not too large.

A die photo of the completed amplifier is shown in Figure 4.20. Since only the top few metal layers are visible it is difficult to see much of the circuit sections. The die size is 772 μm by 822 μm, which fits easily in a standard 8-pin package. For any additional applications of this chip where physical size is even more important, a smaller package can significantly reduce the footprint.

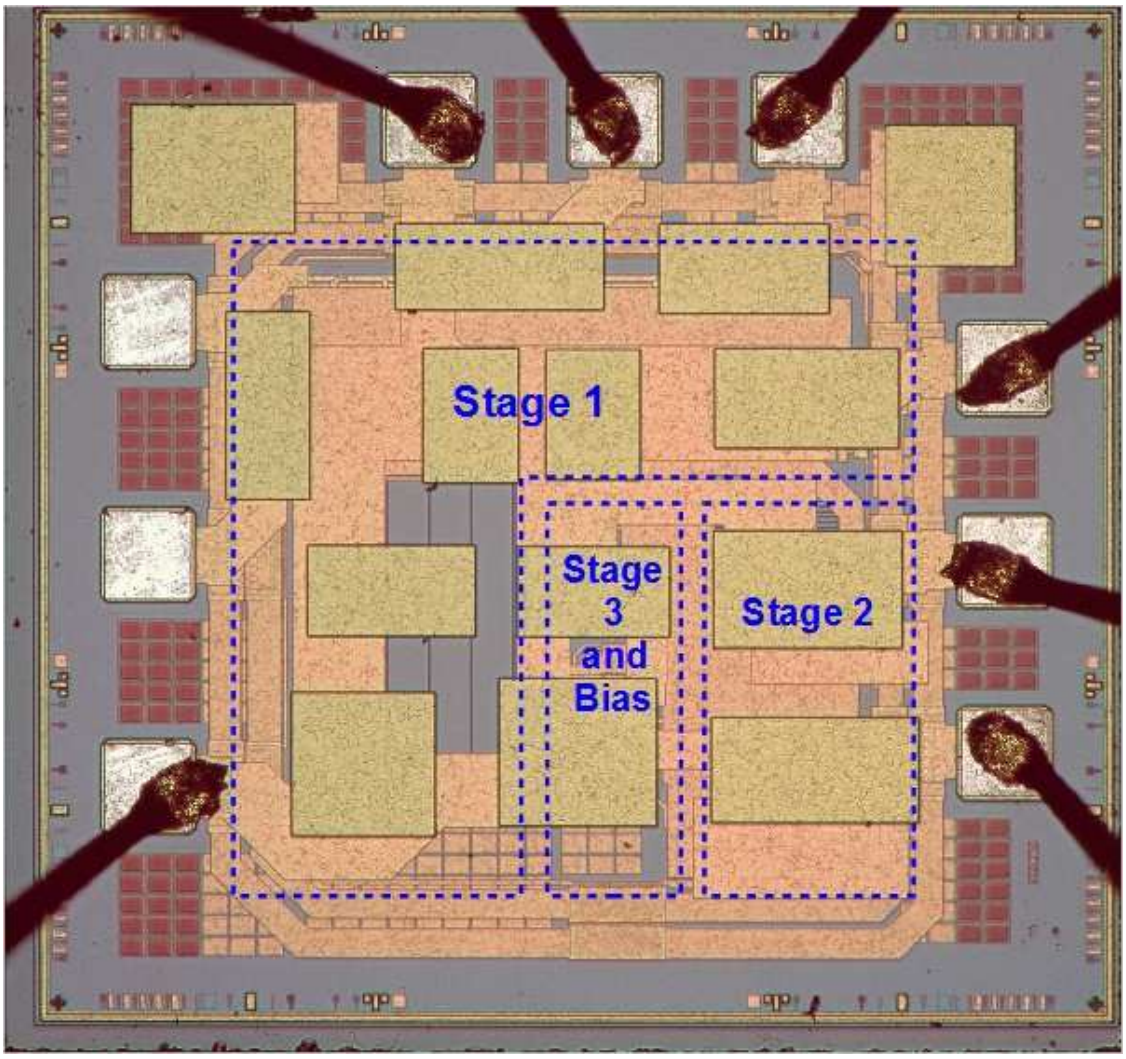

Figure 4.20: Photo of amplifier chip die. Only the top few layers of metal are visible.

Chapter 5

Testing Method

This chapter discusses the testing methods developed for this amplifier. The first Section describes the signal conditioning method to provide the correct input signal. This amplifier is so sensitive that ambient noise that couples in to the wires distorts the output voltage. The output voltage can not be determined simply by viewing an oscilloscope, thus processing is needed to remove the ambient noise and determine the correct measurement and is described below. Finally, the complete test setup that produced the measurements shown in the results chapter is presented.

5.1 Signal Injection

The amplifier requires a balanced differential input signal centered at 0 V DC. Additionally, the signal must be very small (microvolts), and for results that would apply to the system as a whole, be injected with a complex, low impedance source. Function generators produce signals down to only millivolts with either 50 Ω or very high impedance, so some signal conditioning is required for testing. One way to inject the proper signal is to connect the antenna and transformer to the amplifier, and then place the antenna in a appropriate magnetic field. However, it is impractical to produce a known illuminating field that is constant across the span of the antenna. Additionally, the very sensitive antennas pick up so much environmental noise (especially from power lines), that the amplifier is always in saturation when it is connected

to the antenna in any lab environment.

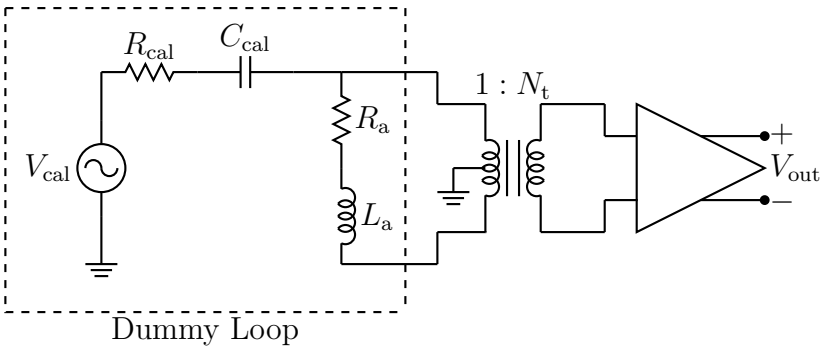

Figure 5.1: Test setup using dummy loop instead of antenna. Components R_{a},L_{a},R_{cal}, and C_{cal} are all part of the dummy loop. The V_{cal} signal is provided by a function generator and should have a high output impedance.

A better approach is to use a dummy antenna which has the same impedance as the antenna but no collecting area. Figure 5.1 shows the dummy antenna design used for testing and how it is connected to the amplifier. The antenna impedance is provided by R_{a} and L_{a}, while R_{cal} and C_{cal} are chosen by the following derivation.

The current flowing to the amplifier (i.e. from the secondary of the transformer) from the source V_{cal} is:

$$I_{\mathrm{in}} = \frac{V_{\mathrm{cal}}}{2R_{\mathrm{cal}}\left(1 + \dfrac{f_{\mathrm{cal}}}{jf}\right)} \left[\frac{j2\pi f L_{\mathrm{a}} \left(1 + \dfrac{R_{\mathrm{in}}}{j2\pi f L_{\mathrm{a}}}\right)}{R_{\mathrm{a}} + j2\pi f L_{\mathrm{a}} + Z_{\mathrm{p}}} \right] \tag{5.1}$$

where

$$f_{\mathrm{cal}} = \frac{1}{2\pi R_{\mathrm{cal}} C_{\mathrm{cal}}}$$

and Z_{p} is the impedance on the primary side of the transformer looking into the

amplifier. The current produced by the antenna voltage V_{a} is:

$$I_{\mathrm{in}} = \frac{V_{\mathrm{a}}}{R_{\mathrm{a}} + j2\pi f L_{\mathrm{a}} + Z_{\mathrm{p}}} = \frac{j2\pi f N_{\mathrm{a}} A_{\mathrm{a}} B}{R_{\mathrm{a}} + j2\pi f L_{\mathrm{a}} + Z_{\mathrm{p}}} \tag{5.2}$$

If these two input currents are equated, the relation between V_{cal} and V_{a} is found:

$$V_{\mathrm{cal}} = \frac{2N_{\mathrm{a}} A_{\mathrm{a}} R_{\mathrm{cal}} B}{L_{\mathrm{a}}} \left[\frac{1 + \dfrac{f_{\mathrm{cal}}}{jf}}{1 + \dfrac{2\pi L_{\mathrm{a}}}{jf R_{\mathrm{a}}}} \right] \tag{5.3}$$

If C_{cal} is chosen as follows:

$$C_{\mathrm{cal}} = \frac{L_{\mathrm{a}}}{R_{\mathrm{a}} R_{\mathrm{cal}}} \tag{5.4}$$

and (2.5) is used to replace V_{a}, the relationship between V_{cal} and an equivalent magnetic field can be found.

$$V_{\mathrm{cal}} = \frac{2N_{\mathrm{a}} A_{\mathrm{a}} R_{\mathrm{cal}} B}{L_{\mathrm{a}}} \tag{5.5}$$

Note that all of the terms with Z_{p} have dropped out, resulting in a simple calibration method that does not require any knowledge of the impedance of the transformer and amplifier. Only the impedance and area of the antenna are relevant. Since the frequency dependencies have dropped out as well, a simple multiplication converts between the input signal and the equivalent field for any antenna. The result is a compact signal conditioning method that uses a standard function generator. This method also can be used for calibration in the field during deployment and maintenance, which allows the users of the data to know how much field the output recorded voltages correspond to.

5.2 Detecting Signals in the Presence of Strong Noise

A direct measurement of the output voltage of the amplifier can not be made in a typical lab environment with an oscilloscope because the presence of large interference from 60 Hz power lines and its harmonics that dominate the waveform. As long as the 60 Hz contamination does not saturate the preamplifier, a narrow-band signal magnitude can still be measured in the frequency domain. To do so, the output signal is first recorded and then transformed to the frequency domain with a Fourier transform and appropriate windowing. The magnitude of the signal at the test frequency is found, and then converted back to voltage. This method allows the measurement to disregard the signal power in other frequencies which represent ambient noise.

The accuracy of this method can be greatly improved by using a suitable window. When a rectangular window is used, it produces a broadband response (with a sinc function shape) in the frequency domain, distorting the results. Instead, multiplying a time data record by a Gaussian window of suitably chosen width produces, in the frequency domain, a Gaussian convolved with the Fourier transform of the unwindowed signal. This Gaussian response in frequency, when represented as the log of the amplitude, becomes a simple quadratic function of the frequency. Fitting a quadratic to the log of the amplitude response affords a simple and robust means of accurately estimating both the frequency and amplitude of the frequency domain response.

The implementation of this method is done after the testing is completed, and requires only a few seconds of computation for each test frequency. First, the function gausswin is defined as:

$$\text{gausswin}(x, \alpha) = e^{-\frac{1}{2}(\alpha x)^2} \tag{5.6}$$

where the standard deviation is the inverse of α. The Fourier Transform of the gausswin function is then:

$$F(\text{gausswin}) = \frac{\sqrt{2\pi}}{\alpha} e^{-2\left(\frac{\pi f}{\alpha}\right)^2} \tag{5.7}$$

In the frequency domain, the Gaussian becomes another Gaussian with a standard deviation of α and magnitude $\sqrt{2\pi}/\alpha$. In order to produce a Gaussian with a unity magnitude in the frequency domain the inverse of this factor should be multiplied in the time domain. This scaling assures that the multiplication by the Gaussian does not attenuate the magnitude in the frequency domain.

$$F(V_{\text{out}}) = \frac{\alpha}{\sqrt{2\pi}}\text{gausswin}(N, \alpha) \tag{5.8}$$

where N is the number of points that will be used in the Fourier transform. After this Gaussian window is multiplied by the recorded data, an N point fast Fourier transform (FFT) is taken. The transformed signal is squared (to convert to a normalized power) and then converted to dB.

To find the magnitude of the peak of the signal in the frequency domain, the three largest points around the maximum are selected, shown by the black "x" inside the box indicating data points in Figure 5.2. The power of the lowest frequency of the three points is assigned α, the actual maximum is β, and the last is γ. The following two equations are then used to estimate the true magnitude of the peak.

$$df = \frac{1}{2}\frac{\alpha - \beta}{\alpha - 2\beta + \gamma} \tag{5.9}$$

$$\text{Peak Magnitude} = \beta - \frac{1}{4}(\alpha - \gamma)df \tag{5.10}$$

This magnitude, shown as a red cross in Figure 5.2, is then converted back to linear scale from dB. To find the final voltage the result must be multiplied by a factor of four involving two factors of two. The first factor of two accounts for the Fourier Transform's factoring the signal in half between positive and negative frequencies, and the second factor of two converts from amplitude to peak-to-peak because the output is a differential signal.

This method was verified by taking data with an alternate, known system at high enough frequencies that the 60 Hz and harmonics did not significantly distort the oscilloscope view of the output waveform. The voltage was measured on the oscilloscope, and then the above calculations were performed for comparison.

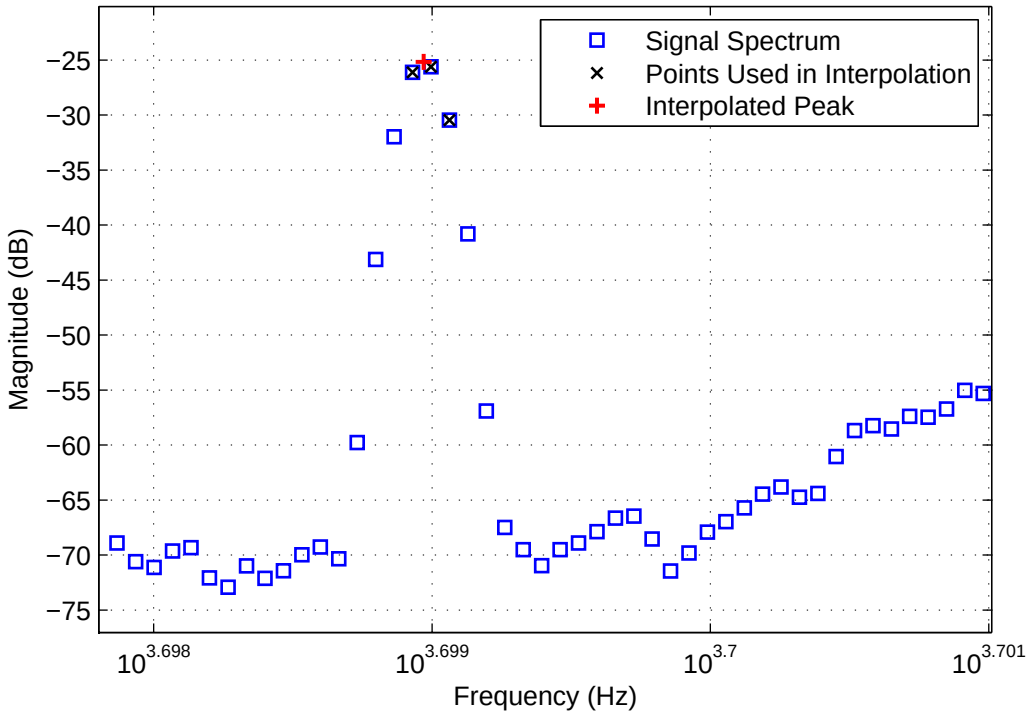

Figure 5.2: Example interpolation of data in the frequency domain. The data points are represented by blue squares. The three points used for the interpolation are marked by a black "x" and the interpolated maximum is marked by the red "+".

In order for this method to work the frequency bin size (f_s/N, where N is the number of points in the FFT) must be small enough to sample the quadratic peak in the frequency domain with enough points for the quadratic interpolation. In the measurements done for this project, a minimum of 6 samples on the frequency peak is retained to ensure the necessary accuracy. Since the bandwidth of this amplifier covers several decades, the sampling rate must be adjusted to ensure that both data is recorded for a long enough time, and that N is large enough. To further improve accuracy, four Fourier Transforms of were averaged together for each measurement to lower the noise floor and remove any small time varying fluctuations. Additionally, large spurs (normally from power harmonics) distort the expected quadratic shape and invalidate the measurement. It is important to look over the spectrum during

testing and choose frequencies in quieter regions.

5.3 End-to-End Test Setup

The main problem for the test setup for this amplifier is the ambient noise coupling into the signal path. Even with the use of a dummy loop instead of an antenna, the amplifiers saturate without any injected signals. Power line harmonics are the largest contributors, but there is also noise from other electronics in the lab and rest of the building.

To keep power line harmonics from being injected directly into the amplifier, the amplifier is powered from a set of small batteries instead of an switching power supply. The signal is captured and recorded by a National Instruments DAQ card, and stored in a computer for the processing described in the previous Section.

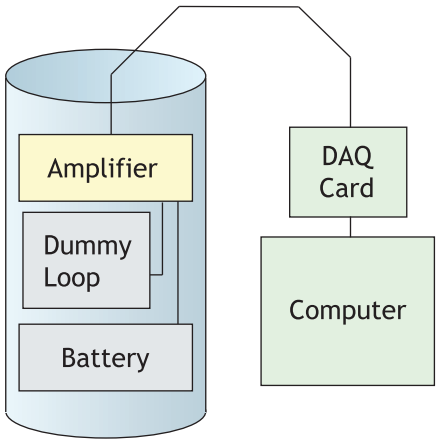

Figure 5.3: Block diagram of testing setup. The amplifier, dummy loop, and batteries are all placed in a three layer mu-metal can for magnetic shielding. The DAQ card and computer capture and store the data for processing.

The amplifier must also be shielded to limit the ambient noise. Because the wavelengths at these low frequencies is so large (power line harmonics are in the 100 km–1000 km range) and the electromagnetic attenuation takes several wavelengths [4, p. 370], a simple Faraday cage will not provide enough shielding for the magnetic field.

Instead, a three layer mu-metal container, which has a large permeability, is used to shield the dummy loop, batteries, transformer, and amplifier from the magnetic field. This can is conductive both electrically and magnetically, and achieves 87 dB of attenuation. For the most sensitive noise measurements, the can must also be kept away from power outlets, people, and other electronics as much as possible. The complete testing setup is shown in Figure 5.3.

Chapter 6

Measured Amplifier Performance

The measured results of the fabricated amplifier are presented here, and are also compared with the specifications. All the tests used the methods described in the previous chapter.

6.1 Power Consumption

The power consumption requirement is important in order to ensure the system has enough power to continue operating for a full year on batteries. The measured current is 1.92 mA, which at a 2.5 V supply results in a 4.8 mW power consumption. This result is below the 5 mW specification, and leaves a small buffer for unexpected variations.

6.2 Gain and Frequency Response

The gain of the amplifier was measured using the setup described in the previous chapter. The results, shown in Figure 6.1, are compared with the simulation. The rolloff at low frequencies is an artifact of the testing setup. The transformer's response rolls off at 300 Hz and below this point very little of the injected signal passes through to the secondary (see Section 2.2.1), causing an apparent reduction in the gain of the amplifier even though its response is flat down to DC. The simulation's representation

of the antenna and transformer causes the simulated rolloff to have a different shape than the measured results. Since both the injected signal and the output signals are decreasing rapidly, the gain ratio begins to approach a zero/zero condition and produces a noisy result. There is good matching midband, with a gain of 0.035 V/nA so the needed gain of 0.015 V/nA was achieved. The high frequency 3 dB rolloff is at 230 kHz, which is much larger than the 30 kHz needed by this project.

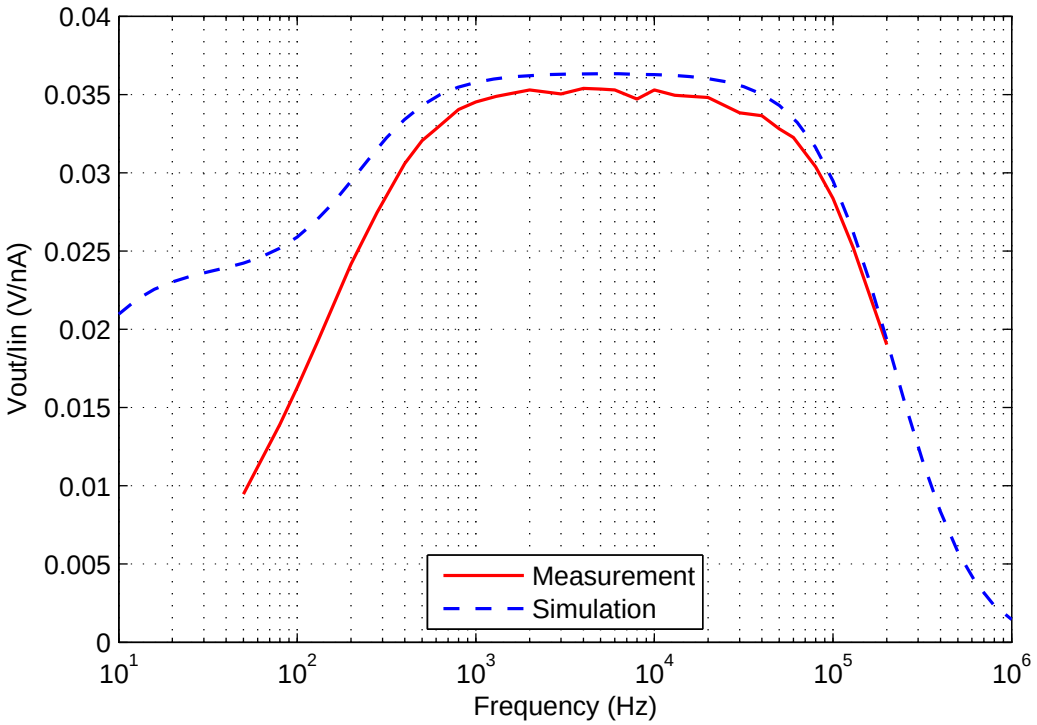

Figure 6.1: Measured current gain compared with simulation.

In order to make sure this amplifier has the correct gain and response for the system as a whole, the response of the system with the antenna is shown in Figure 6.2. The measured and simulated gains match very well across the band, and the measured system gain is 0.275 V/pT.

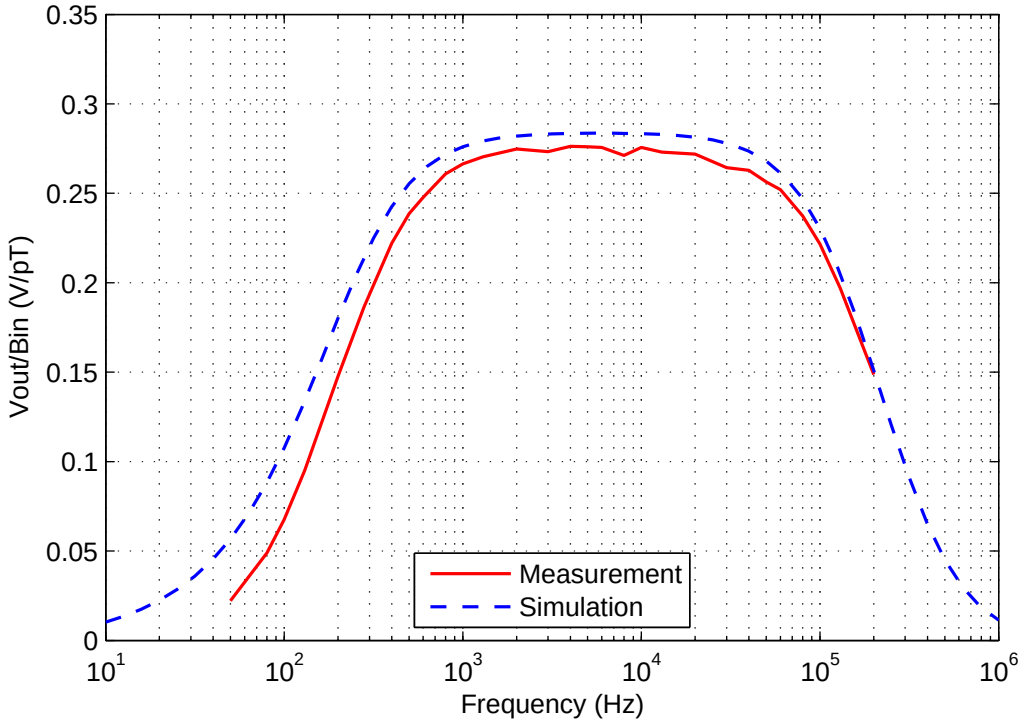

Figure 6.2: Measured gain of antenna, transformer, and amplifier together compared with simulation. The antenna is a five turn triangular antenna with a 10 m base.

6.3 Noise and Sensitivity

The first step when performing these measurements is to record the output noise with no injected signal. The output noise is then referred back to the input, and the contribution of the antenna resistance is removed to leave only the noise of the amplifier, shown in Figure 6.3. The data is averaged four times to reduce the variance, and then a low pass filter is used to remove the large spurious noise peaks, most of which come from power line harmonics. The measured noise remains below the 7.8 pA/$\sqrt{\text{Hz}}$ specification between 200 Hz and 363 kHz, and reaches 2 pA/$\sqrt{\text{Hz}}$. The bandwidth of the noise is determined by the gain response, so the rolloffs correspond to the gain rolloffs in the previous Section.

The system sensitivity is determined by assuming an antenna and referring the

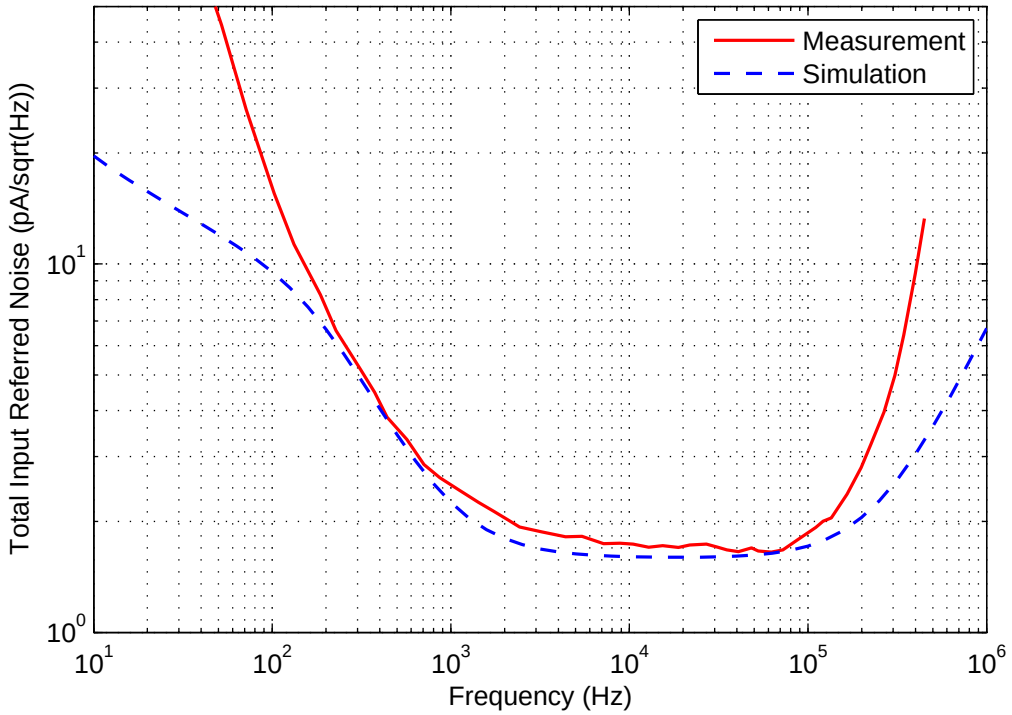

Figure 6.3: Measured current noise referred to the input of the amplifier compared with simulation. The data has been averaged four times and low pass filtered to remove spurious noise peaks.

noise back to the input field. Again the five turn, 10 m base triangular antenna is used, and the results can been seen in Figure 6.4. The sensitivity represents the smallest signals that the system can detect, and for this design, it remains below the 1 fT/$\sqrt{\text{Hz}}$ specification from 234 Hz to 370 kHz. The minimum sensitivity it achieves is 0.25 fT/$\sqrt{\text{Hz}}$, so within most of the band of interest, the system is limited by the atmospheric noise instead of measurement noise. The antenna thermal noise is shown in green for reference, and represents the minimum this amplifier can achieve. If further improvement in sensitivity is needed, a larger antenna can be used if the physical space and material weight permitted (as discussed in Section 2.1.1). Although the simulation models the actual performance well in the middle of the bandwidth, it underestimates the noise at the edges of the bandwidth. At low frequencies, the

simulation does not accurately model the $1/f$ noise of the actual fabricated devices. Also the noise at the output of the amplifier decreases rapidly at the bandwidth edges along with the gain, making the noise measurements in these regions less accurate.

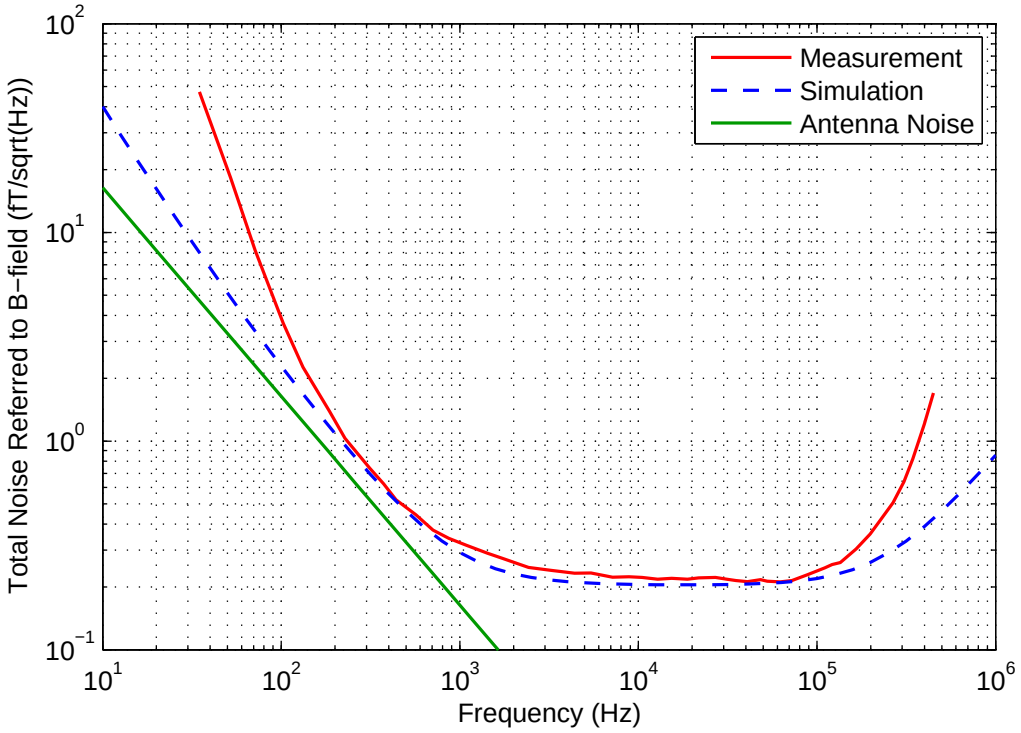

Figure 6.4: Measured sensitivity of antenna, transformer, and amplifier together compared with simulation. The antenna is a five turn triangular antenna with a 10 m base. The antenna thermal noise portion of the total noise is shown in green as the lower limit to the system performance.

6.4 Linearity

The linearity is tested by measuring the harmonics of the output signal, and comparing them to the magnitude of the fundamental. The result is called the total harmonic distortion (THD) and is a measure of how much energy is diverted away from the fundamental. The magnitude of the harmonics decreases rapidly with each harmonic

power, so for this testing only the first five harmonics were measured. The equation for determining the harmonic distortion is then:

$$\text{THD} = \frac{V_2^2 + V_3^2 + V_4^2 + V_5^2}{V_\text{f}^2} \tag{6.1}$$

where V_f is the fundamental frequency of the signal that was injected [12, p. 360].

The measured distortion for this amplifier is 57 dB. With a 16 bit ADC, the dynamic range of the system is theoretically $2^n - 1$, or 96 dB. Since the ADC will have some noise, its dynamic range will be slightly lower, closer to 90 dB. The amplifier's dynamic range is less than the ADC, so the amplifier limits the dynamic range of the system as a whole. However, since these distortions only appear with the strongest signals, and decrease dramatically as the input signal is reduced, the data will not be affected unless there is a strong, nearby impulsive signal. Additionally, at higher frequencies, these harmonics will be out of the band of interest, so they will appear only with the strongest signals that occur in the lower half of the bandwidth.

Chapter 7

System Design

The amplifier was incorporated into a full magnetic receiver system intended for deployment in Antarctica. Since the rest of the system must be designed to integrate well with the amplifier in order to meet the system specifications, the remaining portions of the analog front end are discussed further here. The antenna and input transformer designs are discussed in Section 2.3. The amplifier board and the anti-aliasing filter designs are included in the Sections below. The digital and mechanical systems designed by Max Klein [21] were combined with the analog portions, and the full system was then field tested in Antarctica and the results from this test are presented.

7.1 Preamplifier Board

The preamplifier board includes the transformer, amplifier, buffer, and output transformer, as shown in Figure 7.1. Power is supplied by the digital box at 3.3 V. Since the amplifier's supply must stay below 2.5 V, a linear regulator is used to drop the voltage from 3.3 V to 2.5V. Any switching power supply would create too much noise in band, and must be avoided near any of the analog circuitry. Although they are not shown here, it is important to add capacitors to every supply pin on each chip to minimize the low frequency noise on the power line from leaking into the signal path. The diodes (D_1 and D_1) at the input of the amplifier protect the chip from damage

from large input signals and any accidental temporary shorts during handling and deployment.

After the custom amplifier chip, the two low noise opamps (AD8086) provide the required current to drive the transformer and long cable without slewing. Capacitors C_4 and C_5 are used to limit the bandwidth of the op-amp circuits to improve stability. The output transformers were also custom made to ensure their quality. The transformer steps down the impedance with a turns ratio of 3:1, so that the buffer amplifier can drive the 78 Ω cable. It also provides electrical isolation from the cable and digital box. The output capacitors C_6 and C_7 roll off the gain below 48 Hz, and protect the chip against any slight imbalance in output DC current. Since there are two channels (with the antennas set up orthogonally to detect waves from any direction), each board has two copies of this circuit.

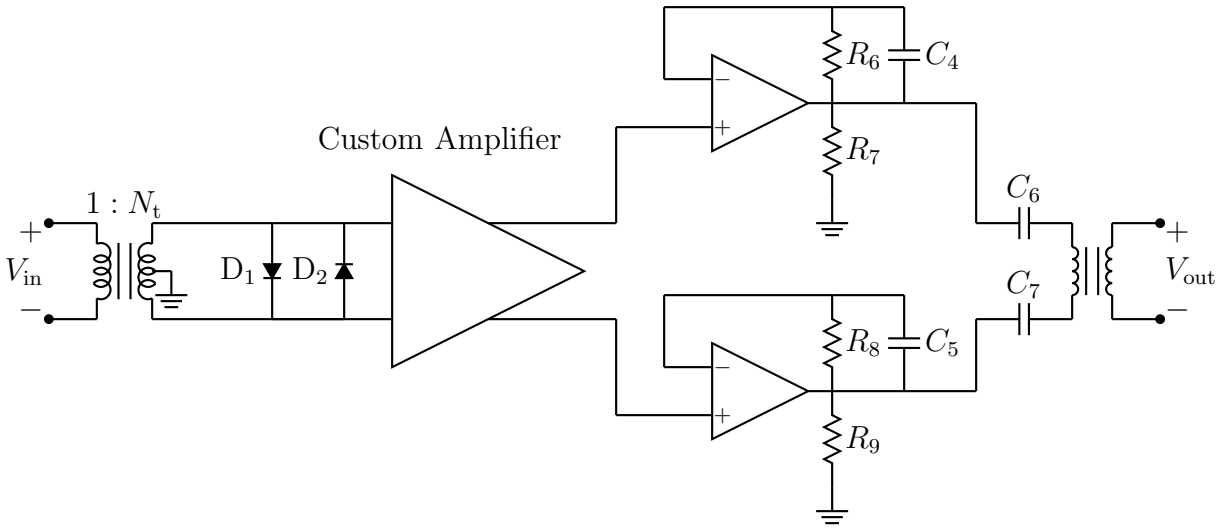

Figure 7.1: Simplified schematic of preamp board. Power supply regulation and capacitors are not shown. Each board has two copies of this circuit, one for each channel.

The final board is shown in the photograph in Figure 7.2. To conserve space, one channel was placed on each side of the board. The board is 2.75 inches wide by 5.75 inches long, with a total height of 3.0 inches. To keep it warm, the board was placed within two layers of 0.5 inch insulation with an R-value of 3.18 m^2K/W each,

and protected with an aluminum box. The final box has two antenna connectors, and a single cable that connects to the digital box. The final version of the box assembly is 10 inches by 12.25 inches by 5.75 inches, but can be reduced in size, as long as the insulation thickness remains the same.

Figure 7.2: Photo of preamp box including preamp board and insulation. Each box includes two analog channels.

7.2 Anti-Aliasing Filter

The filter board is located in the digital box, and provides the anti-aliasing filter before the signal is digitized. The filter shown in Figure 7.3 is on a separate board from the rest of the digital electronics to minimize noise coupling into the analog signal before digitization. Additionally, the separate filter board allows for easy replacement with a new filter if a different bandwidth or response is needed for a particular application,

with no need to change the rest of the digital board. The 78 Ω load resistance (R_1) terminates the 78 Ω cable without causing reflections. The two resistors R_2 and R_3 are large and provide some isolation from the long cable. They also allow resistors R_4 through R_7 to set the DC level. The diodes provide protection from any large signal accidentally connected to the board. Next, the Op-Amps OP1, OP2, and OP3 (AD8606) are in an instrumentation amplifier configuration in order to convert to a single ended signal and drive the filter, which has a large reactive impedance. This instrumentation amplifier is also a convenient location where the system gain can easily be adjusted by simply changing the resistors R_8, R_9, and R_{10}.

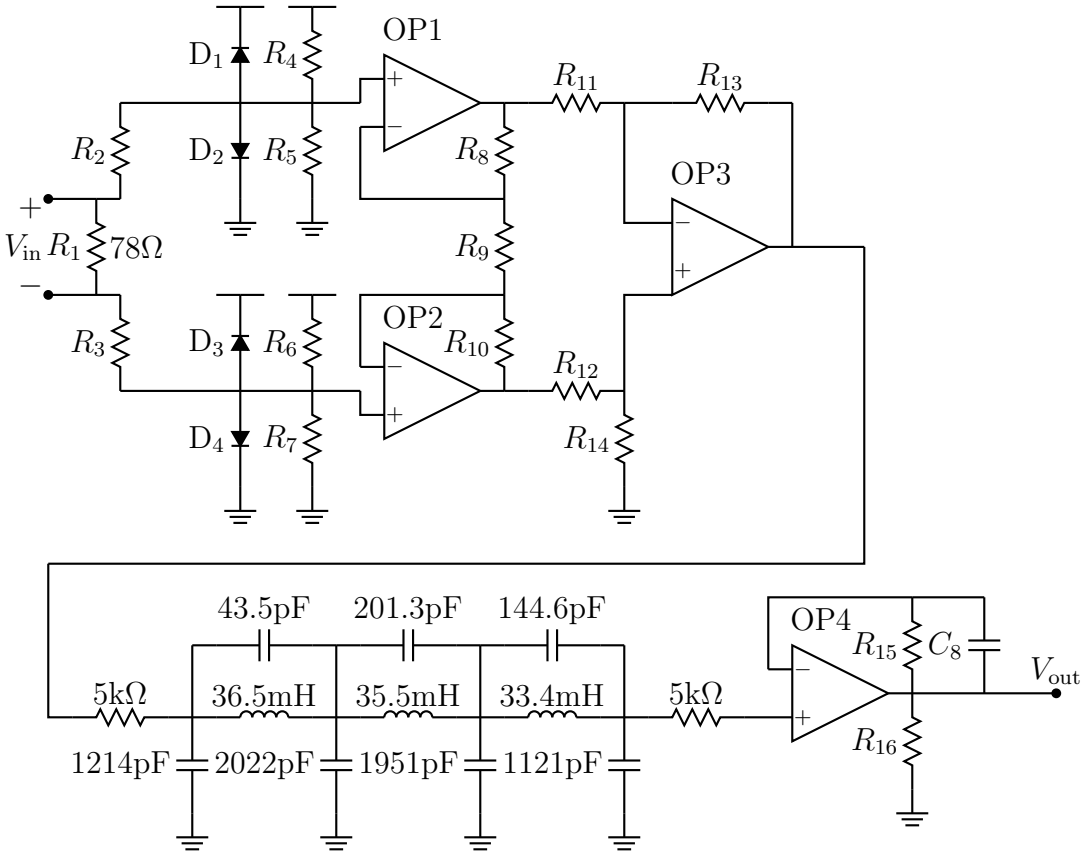

Figure 7.3: Simplified schematic of filter board. Power supply regulation and capacitors are not shown. The ideal values for the filter components are shown for reference. Each board has two copies of this circuit, one for the signal from each antenna.

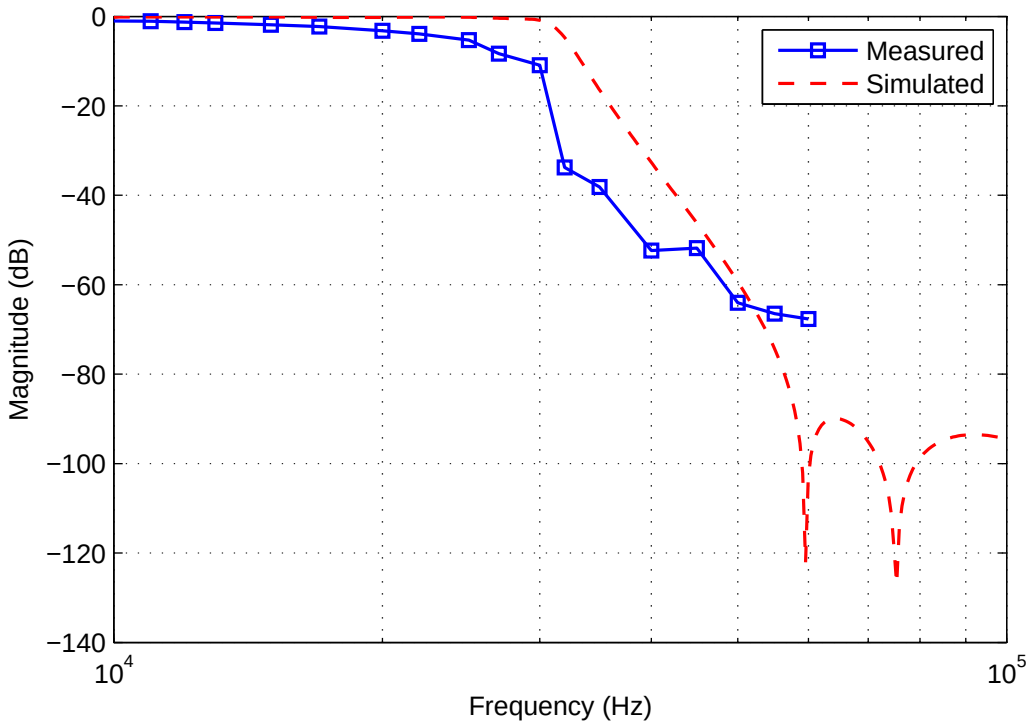

Figure 7.4: Simulated and Measured Filter Response. Measurement equipment is limited to -70 dB, so data can not be collected past that point.

The filter is passive in order to save power and is a 7th order Cauer (elliptical) with a rolloff at 30 kHz. It must reduce the gain to the noise floor by half the sampling rate in order to prevent aliasing during sampling from contaminating the data. With a sampling rate of 100 kHz, if the filter response is down about 90 dB by 70 kHz, the aliasing will affect the data only above 30 kHz, which is outside the bandwidth desired for the receiver. The ideal component values are shown in Figure 7.3. However, it is very difficult to control the capacitance and inductance of these parts to the tolerance required to ensure the response meets the requirements, so each filter must be individually tuned by measuring the actual component values until the correct combination is found.

The simulated and measured response are shown in Figure 7.4. Because the measurement equipment is limited to -70 dB, the response below that point could not

be measured. The measured rolloff is not as steep as the simulated, and the 3 dB point is at 20 kHz instead of 30 kHz as shown in Figure 7.5. Although further tuning can improve the response somewhat, small parasitic resistances in the connections, board traces, and especially the large inductors will continue to degrade the performance.

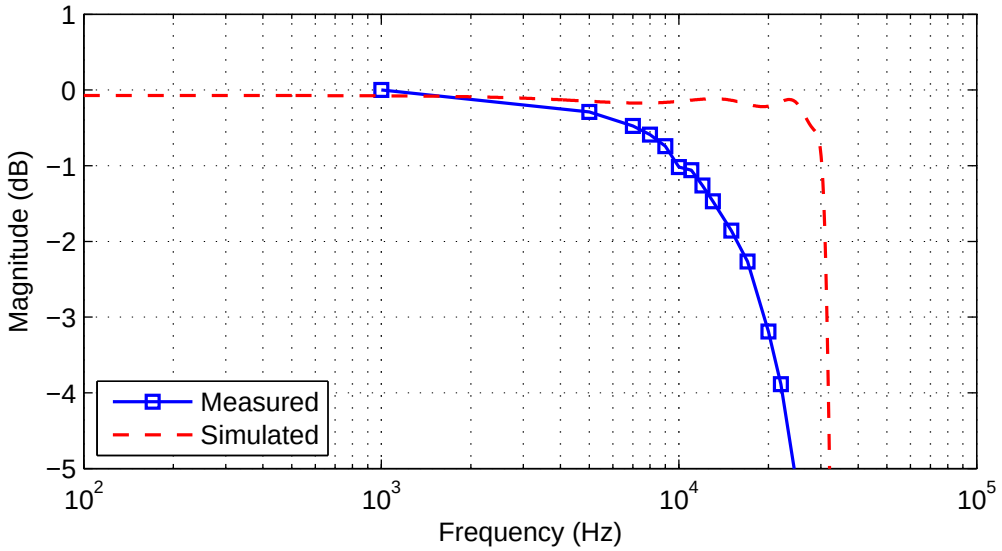

Figure 7.5: Simulated and Measured Filter Response, zoomed in to the 3 dB point. The roll off is at 20 kHz.

A small buffer after the filter (OP4) provides the needed current to drive the ADC, while minimally loading the filter. The capacitor C_8 rolls off the gain at high frequencies to minimize the noise bandwidth of the ADC. The ADC (AD7687) is a 16 bit differential converter with a 93 dB signal-to-noise-and-distortion (SINAD) ratio. This large SINAD means that the ADC is not limiting the performance of the system.

The board size is 6 inches by 6 inches which is much more room than is required by the filter for both channels. The size of the filter board is set to match the digital board so that they can stack together easily. The filter board and digital boards are joined together and surrounded by 1 inch of insulation with an R value of 6.4 m^2K/W. This insulated box is then installed above the battery pack, and the assembly is surrounded by another 2 inches of insulation. The batteries weigh about 10 lbs and are included in the second layer of insulation because they are more

efficient and last longer when they are warmer than the −55°C ambient temperature. The full assembly is shown in Figure 7.6, and the box is 12 inches by 12 inches and 16 inches high. The system was tested at −55°C in a thermal chamber in the lab before deployment. The main issue that was raised during the cold testing is the damage that can be done physically to the boards by corrosion due to condensation, often directly affecting the system performance. Although it is cold enough to freeze all water when the system is operating in Antarctica, all the boards are conformal coated to protect them during shipping and deployment.

7.3 Field Test

The system was deployed in Antarctica by Max Klein (a graduate student in the VLF group) in February 2009 at the South Pole [21]. A short test was first performed for ten days with the electronics on the surface of the snow to ensure the system was working. Then the preamplifier box was buried about 4 ft below the surface of the south directly under the antennas, while the digital electronics were buried about 6 ft under the snow. The system was left undisturbed until November 2009, and the data has now been transported back to Stanford for storage and science use.

An example of the data is shown in Figure 7.7. Since the field test was conducted close to the South Pole Station, noise from the generators and electronics is visible in channel 0. Both channels detect a phenomenon called chorus, which are one of the low level signals this project was intended to capture. The field test demonstrated the usefulness of the system, and indicated issues that must be addressed in the final system. The external bias for the amplifier chips make them difficult to set correctly in the field. This problem is easily corrected by using bandgap onchip bias devices, which are readily available. Additionally, there were intermittent digital timing errors which caused portions of the data to be lost. These issues are currently being resolved, and the system is projected to be ready for Antarctica again in the fall of 2010.

Figure 7.6: Photo of digital box, which includes the battery back, digital card with storage, and the filter card. Only the filter card is visible.

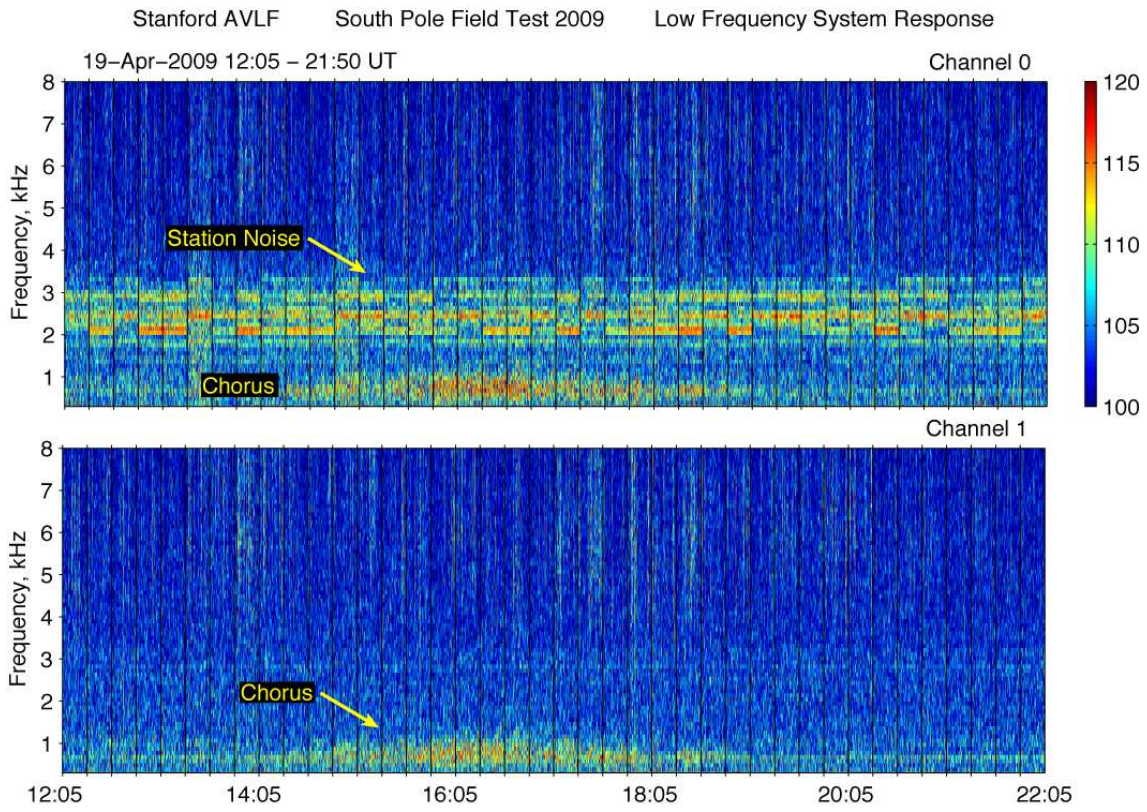

Figure 7.7: Data recorded in Antarctica during field test. The noise from the South Pole station is visible in channel 0, and chorus is observed in both channels.

Chapter 8

Discussion

The main contribution of this work is the demonstration, for the first time, that an amplifier suitable for low frequency magnetic applications can be successfully integrated on a chip. Additionally, the amplifier successfully achieves the noise requirements of 7.8 pA/$\sqrt{\text{Hz}}$ between 200 Hz and 363 kHz and a gain of 35 mV/nA, while remaining below the 5 mW power consumption requirement. During the design work, a new noise optimization method was developed for the common-base topology, which has general application in improving the noise performance in designs with different requirements.

The amplifier was successfully integrated in an autonomous magnetic receiver system and field tested in Antarctica. The recorded data has excellent examples of manmade transmitters as well as common atmospheric phenomenon such as spherics and chorus, demonstrating that the system will provide useful data for science research as they are deployed in the coming years.

8.1 Future Work

Any design is never completely finished as there is always new ideas and process opportunities to incorporate. A standard bandgap reference for on-chip biasing would remove potential noise and functionality problems from temperature changes.

It would be interesting to experiment with how much the new low power digital

electronics radiate noise. If the digital box could be close enough that it was combined with the analog circuitry, it would greatly simplify the system, since only a single box would be required. The preamplifier card would no longer need an output transformer, but could instead go directly to the filter card. However, it may be important to thermally isolate the amplifier board, as the irregular power consumption of the digital electronics will cause the internal temperature to cycle. If there is a large thermal change while the system is recording the data, it may affect the amplifier performance.

Linearity remains one of the areas where there could be the most improvement. The most effective strategy would be to introduce feedback to linearize the output stage. Additionally, if access to a BiCMOS or bipolar process that can tolerate a higher supply voltage could be acquired it allowing a larger transistor and more topology options. This change would make the power consumption limit more challenging, but it may be possible to achieve a better performance.

A process that includes PNP bipolar devices would also allow for other improvements. These PNP devices would be used as loads in the first stage which would remove the dependence of the first stage gain and DC level on the resistors that change by 10%. This topology would also greatly increase the gain of that stage, making it possible to remove the second gain stage, and the signal would then go directly to the output stage. These changes would simplify the design, leave more current for the remaining two stages, and reduce the DC level difficulties.

8.2 Other Applications

This system can also be used in any remote location where a power source is not available, merely by reducing the insulation as needed. Signals from lightening and low frequency transmitters can be monitored away from the manmade noise that is prevalent in all inhabited areas. These receivers can be deployed in islands, jungles, high mountains, and even inside a buoy. They can also be easily moved to a new location. In sunny locations the system could charge it's batteries with solar panels, leaving the data storage as the only remaining limitation. As storage and processing power continues to increase with technology advances, these systems could be serviced

even less often.

This low power, low noise amplifier can be used in other applications where a low impedance sensor is used. This chip would work well for handheld magnetometers, where a compact, sensitive amplifier that will maximize battery life is needed. In nerve research in isolated tissue, an array of sensitive amplifiers is needed to detect activity in the cells. This amplifier could be copied multiple times on the same die to create an extremely compact array.

If the process is space qualified, this design can also be used in satellite applications where minimizing the physical size and weight of equipment is critical. A smaller package would reduce the weight further.

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